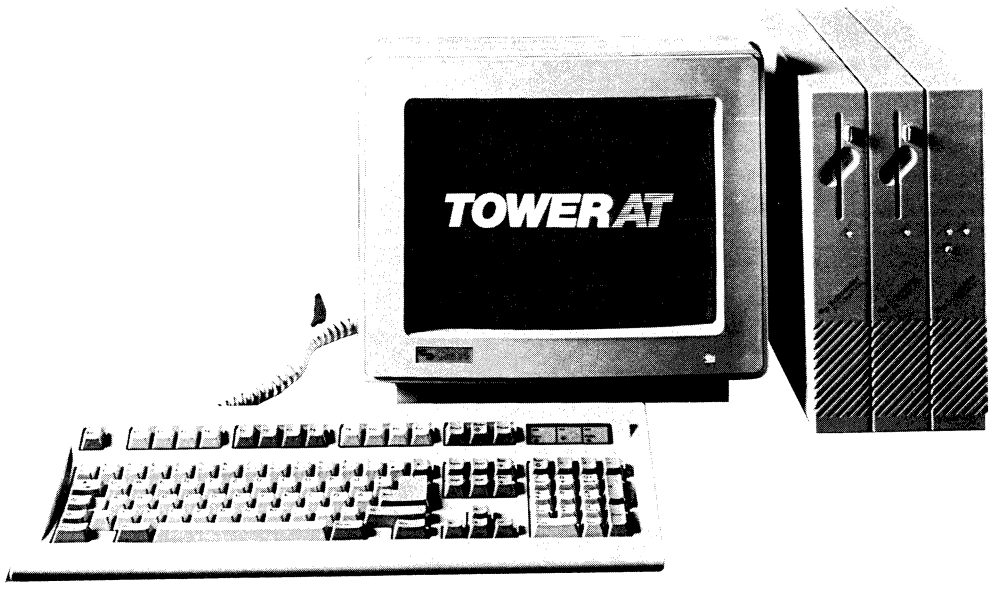
Kundendienst-Handbuch
Service Manual

PERSONAL COMPUTER
Tower AT 201/202/220

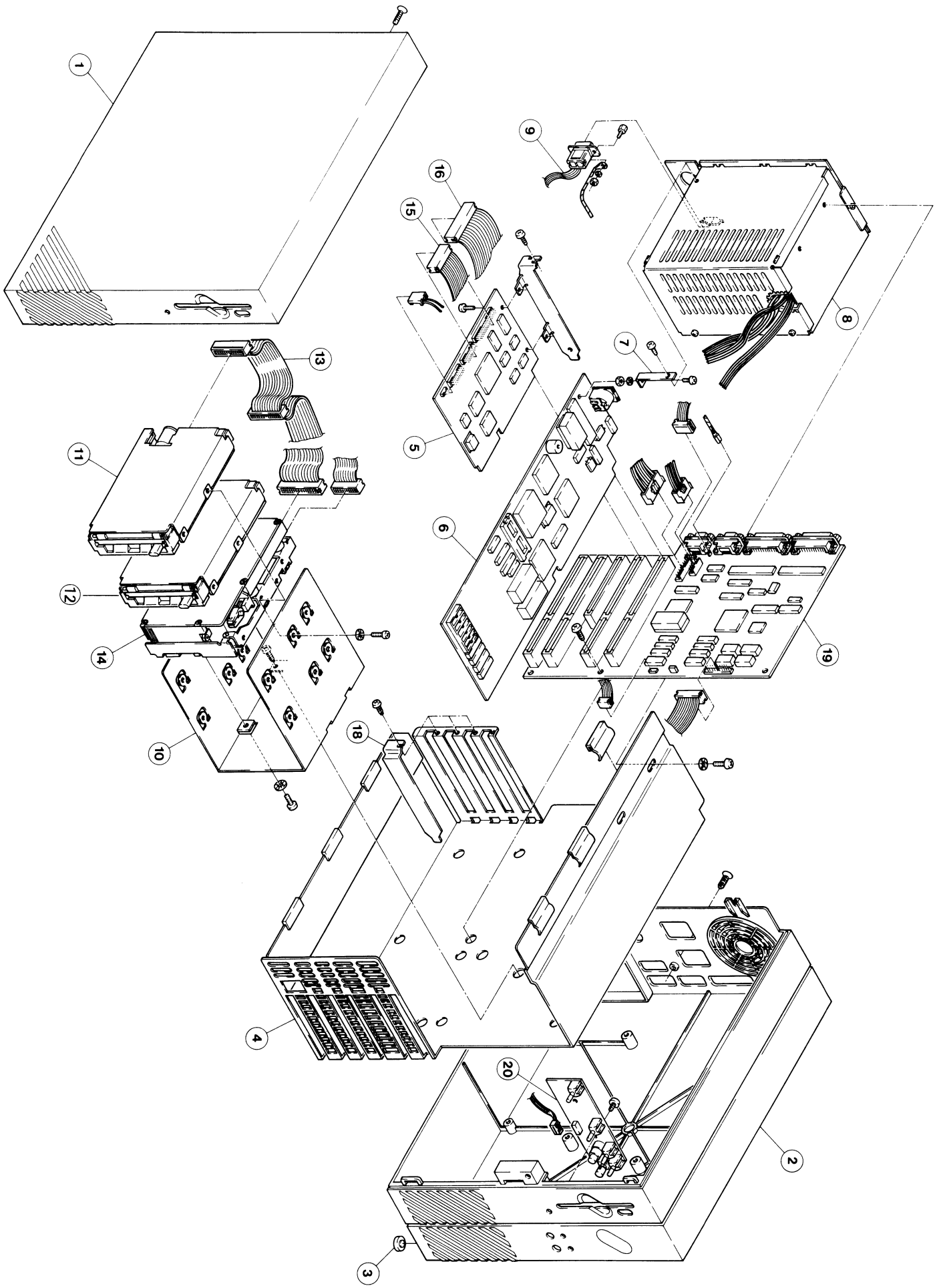


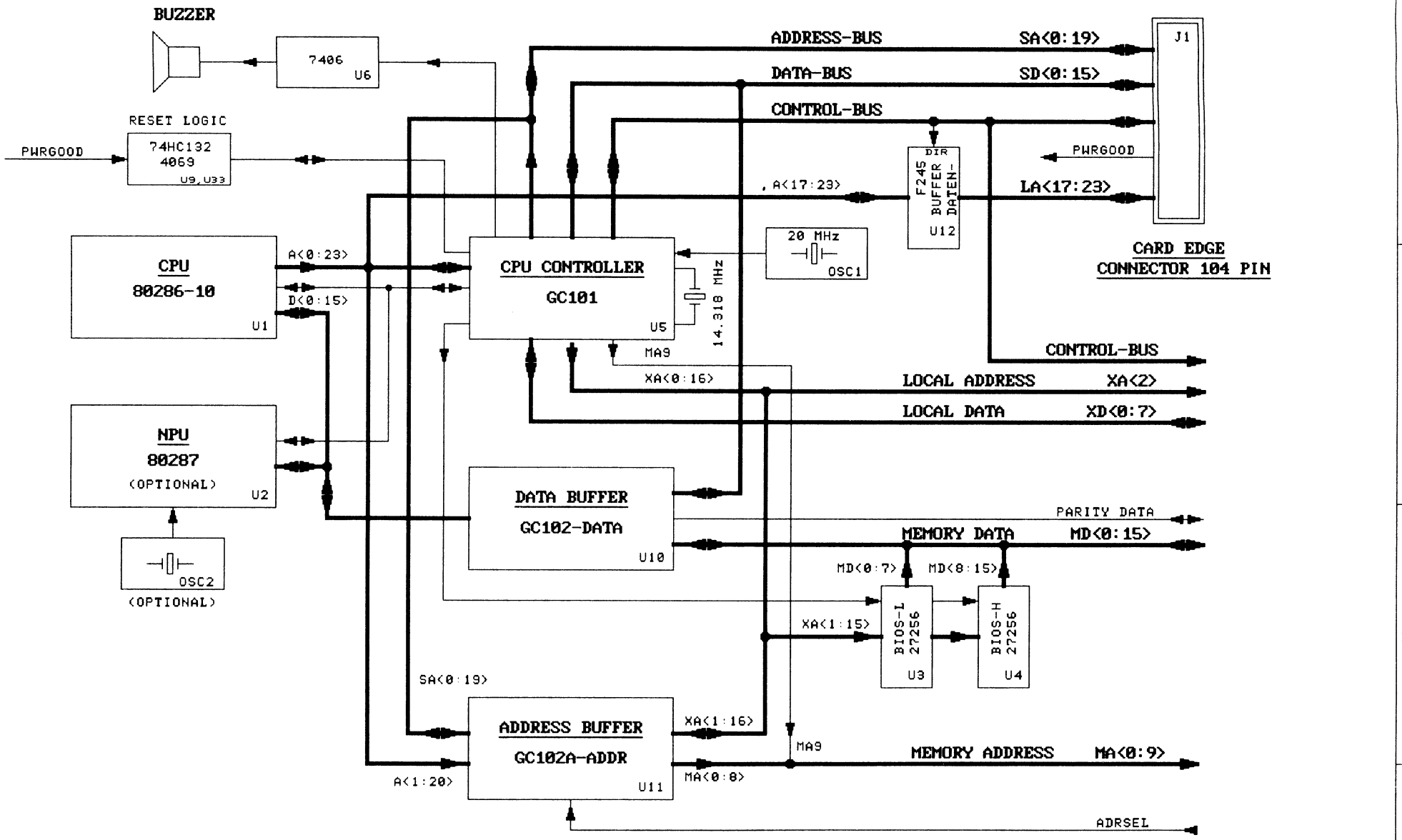
Ersatzteilliste für Tower AT 201/202/220
Parts List for Tower AT 201/202/220

Bestell-Nr. Part.-No.	Bezeichnung	Description	Zeich.-Pos. Ref.-No.	Preisgruppe
50 467 00	FK System Tower	Box system tower		C 3
50 466 00	Sty-Verp. System Tower	Polyfoam system tower		C 3
50 495 00	FK Tastatur Tower	Box keyboard tower		C 2
50 496 00	Sty-Verp. Tastatur Tower	Polyfoam keyboard tower		C 2
50 481 00	Tastatur (D)	Keyboard (D)		F 6
50 482 00	Tastatur (F)	Keyboard (F)		F 6
50 202 00	Tastatur (DK)	Keyboard (DK)		F 6
50 203 00	Tastatur (I)	Keyboard (I)		F 6
50 204 00	Tastatur (N)	Keyboard (N)		F 6
50 485 00	Tastatur (S/SF)	Keyboard (S/SF)		F 6
50 206 00	Tastatur (P)	Keyboard (P)		F 6
50 214 00	Tastatur (GR)	Keyboard (GR)		F 6
50 484 00	Tastatur (GB)	Keyboard (GB)		F 6
50 483 00	Tastatur (E)	Keyboard (E)		F 6
50 486 00	Tastatur (CH)	Keyboard (CH)		F 6
50 097 00	Netzkabel (D)	Cord AC (D)		C 0
50 562 00	Netzkabel (GB)	Cord AC (GB)		C 0
50 617 00	Netzkabel (CH)	Cord AC (CH)		C 0
50 225 00	Gehäuse Oberteil Tower	Cabinet top	1	C 3
50 226 00	Gehäuse Unterteil Tower	Cabinet bottom	2	C 9
50 493 00	Gehäusefuß	Leg	3	A 5
50 172 00	Blechchassis Tower	Chassis metal	4	D 4
50 450 00	HD Controller 220 MFM	HD Controller 220 MFM	5	G 1
50 229 00	Platine Best. (D) Tower AT CPU	PCB (D) tower AT CPU	6	*
50 293 00	Haltewinkel CPU Leiterplatte	Angle CPU	7	A 9
50 215 00	Netzteil Tower 90 W	Power supply tower 90 W	8	G 8
50 448 00	Kabelbaum 9pol.	Cable 9-pol.	9	B 8
50 171 00	Floppyhalter	Bracket floppy	10	B 8
50 472 00	Floppy Laufwerk	Floppy disk drive	11, 12	G 7
50 221 00	Kabelbaum Floppy 26pol.	Cable floppy 26-pol.	13	B 7
50 473 00	Hard Disk Laufwerk	Hard disc drive	14	J 9
50 220 00	Kabelbaum 20pol.	Cable 20-pol.	15	B 9
50 223 00	Kabelbaum 34pol.	Cable 34-pol.	16	C 5
50 224 00	Blindblende	Plate blind	17	A 9
50 020 00	Blindblech	Plate blind	18	B 9
50 228 00	Platine Best. (D) Tower EGA I/O	PCB (D) tower EGA I/O	19	J 1

*Preis auf Anfrage

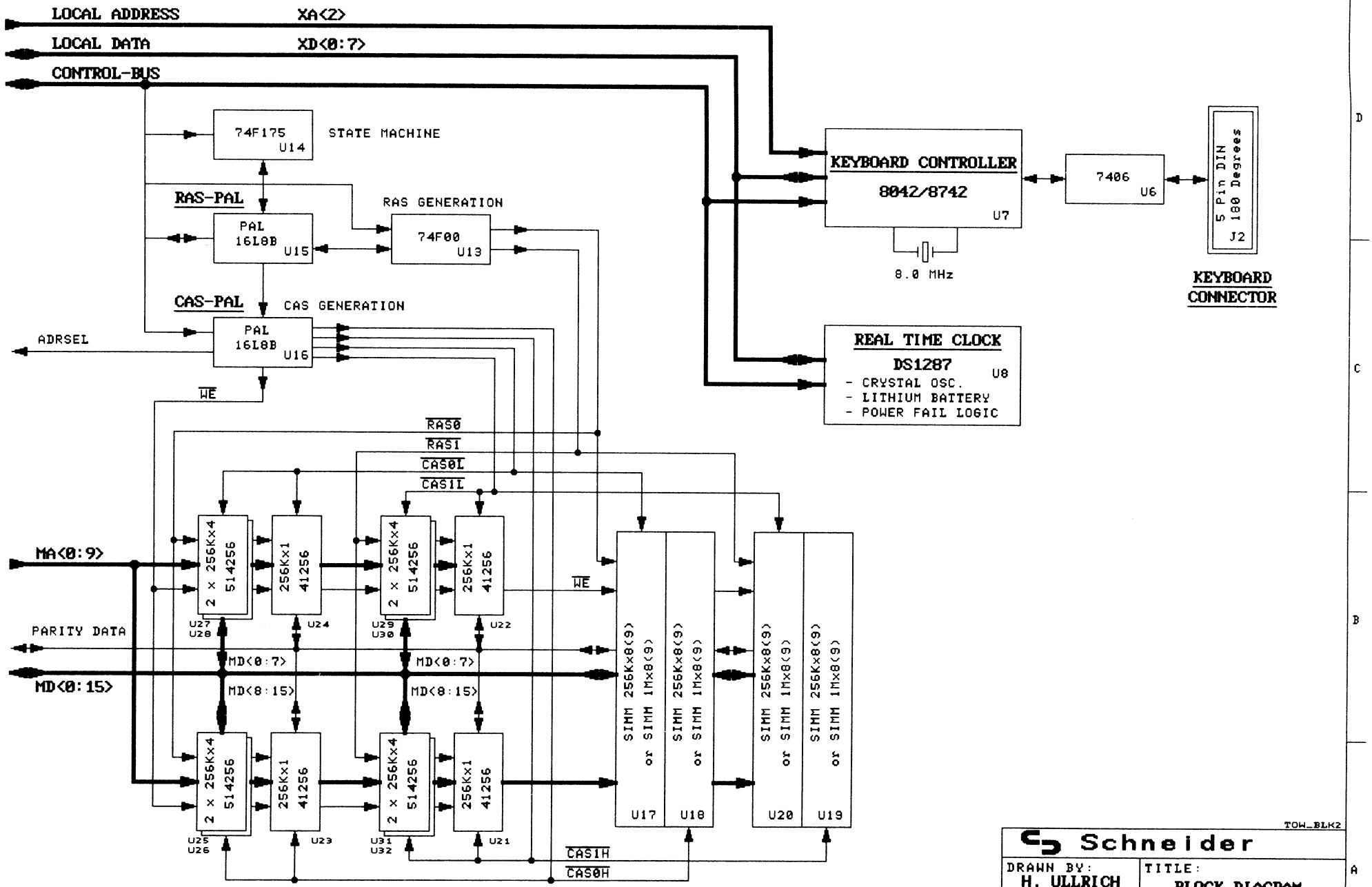
Exploded view





TOW_BLK1

Schneider			
DRAWN BY: H. ULLRICH	TITLE: BLOCK DIAGRAM TOWER CPU286 PCB		
APPROVED:			
USED ON: TOWER AT	SIZE A 3	50 229	REV 1
DATE: 10-05-88	SHEET: 1 of 2		



TOW_BLK2

Schneider

DRAWN BY: H. ULLRICH	TITLE: BLOCK DIAGRAM TOWER CPU286 PCB		
APPROVED:			
USED ON: TOWER AT	SIZE A3	50 229	REV 1
DATE: 10-05-88	SHEET: 2 of 2		

REVISIONS

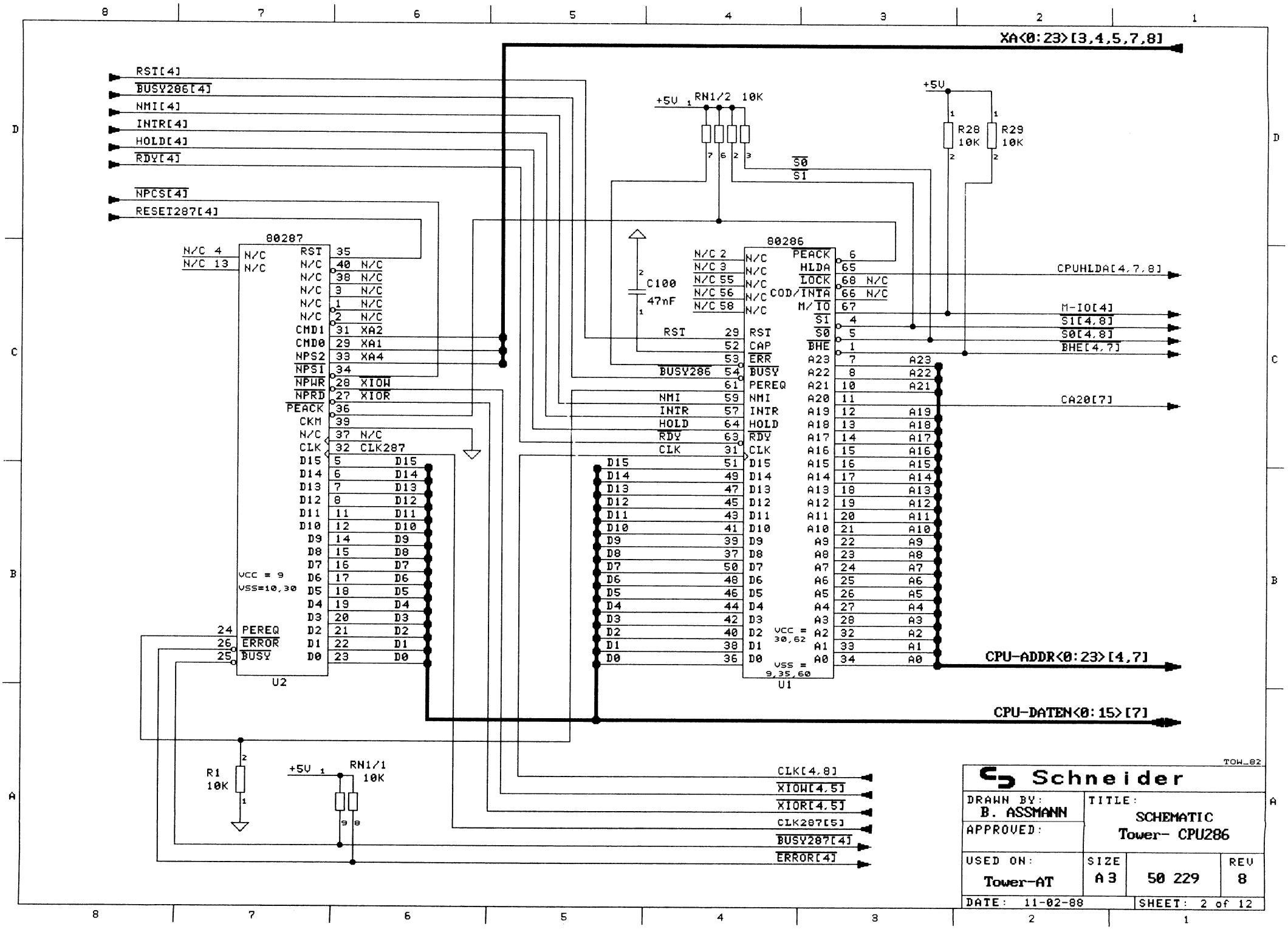
LTR	DESCRIPTION	DATE	APPROVED
1	ADVANCED ENGINEERING RELEASE	05-13-88	SCHLAGE
2		05-18-88	ASSMANN
3		06-01-88	SCHLAGE
4	First Layout	06-22-88	SCHLAGE
5	Layout REV 2	08-06-88	ASSMANN
6	Layout REV 2 CORRECTIONS	08-22-88	ASSMANN
7	PCB REV 2A FIX OF BUS '/MASTER'	08-31-88	ASSMANN
8	PCB REV 4. LAYOUT: ADDITIONAL RESET LOGIC ELIMINATED	10-27-88	ULLRICH

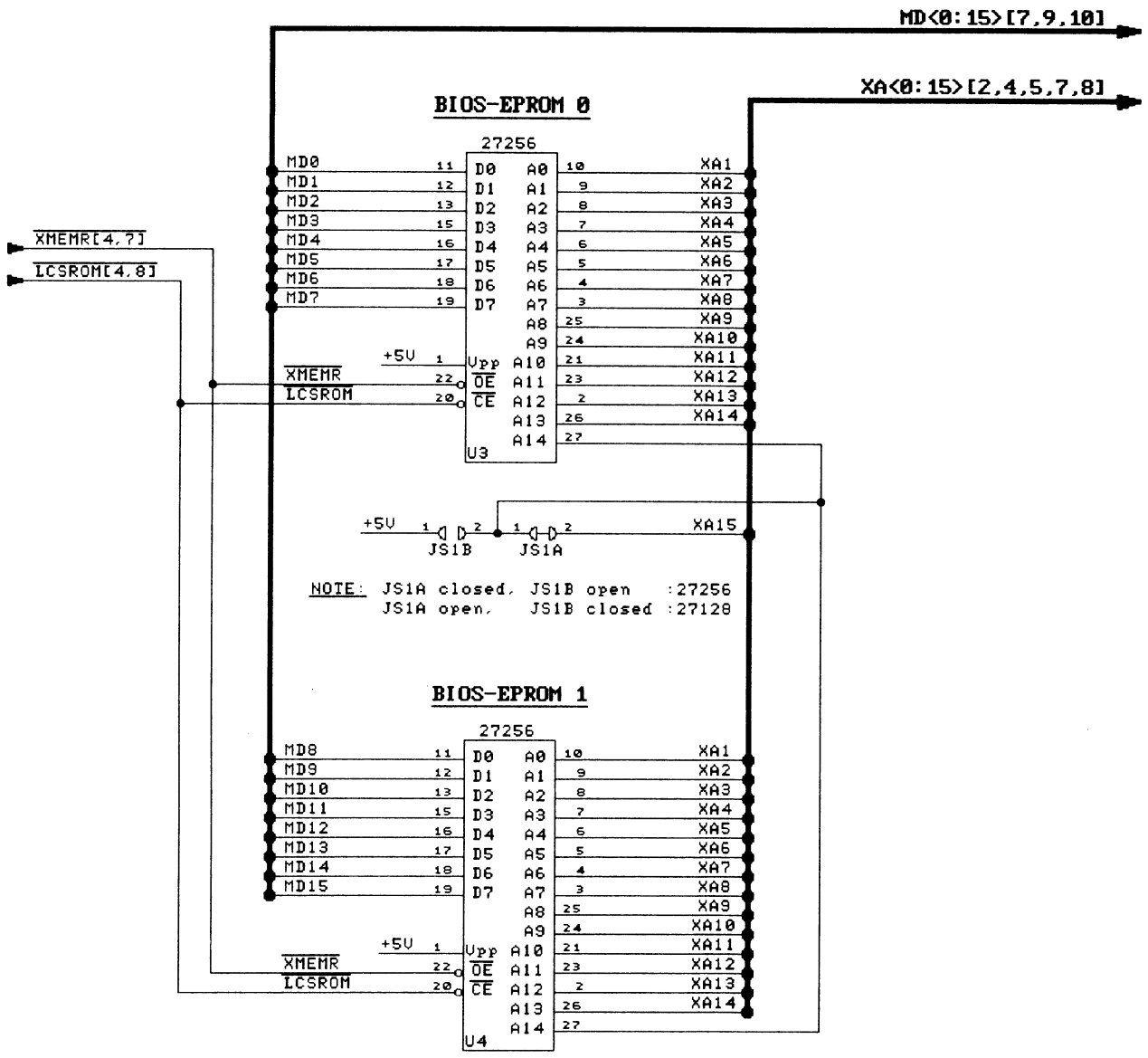
DRAWING FILES:	CONTENTS:
TOW_81.DWG	THIS SHEET
TOW_82.DWG	CPU SECTION
TOW_83.DWG	BIOS EPROMS
TOW_84.DWG	GC101
TOW_85.DWG	KEYBOARD / CLOCKS
TOW_86.DWG	REAL TIME CLOCK
TOW_87.DWG	ADDRESS / DATA BUFFERS
TOW_88.DWG	TIMING FOR MEMORY
TOW_89.DWG	MEMORY ON SIL- MODULE
TOW_810.DWG	MEMORY ON BOARD
TOW_811.DWG	CONNECTORS
TOW_812.DWG	BLOCK CAPS

TOW_81

Schneider

DRAWN BY: H. ULLRICH	TITLE: SCHEMATICS Tower- CPU286		
APPROVED:			
USED ON: Tower-AT	SIZE A3	50 229	REV 8
DATE: 11-02-88	SHEET: 1 of 12		

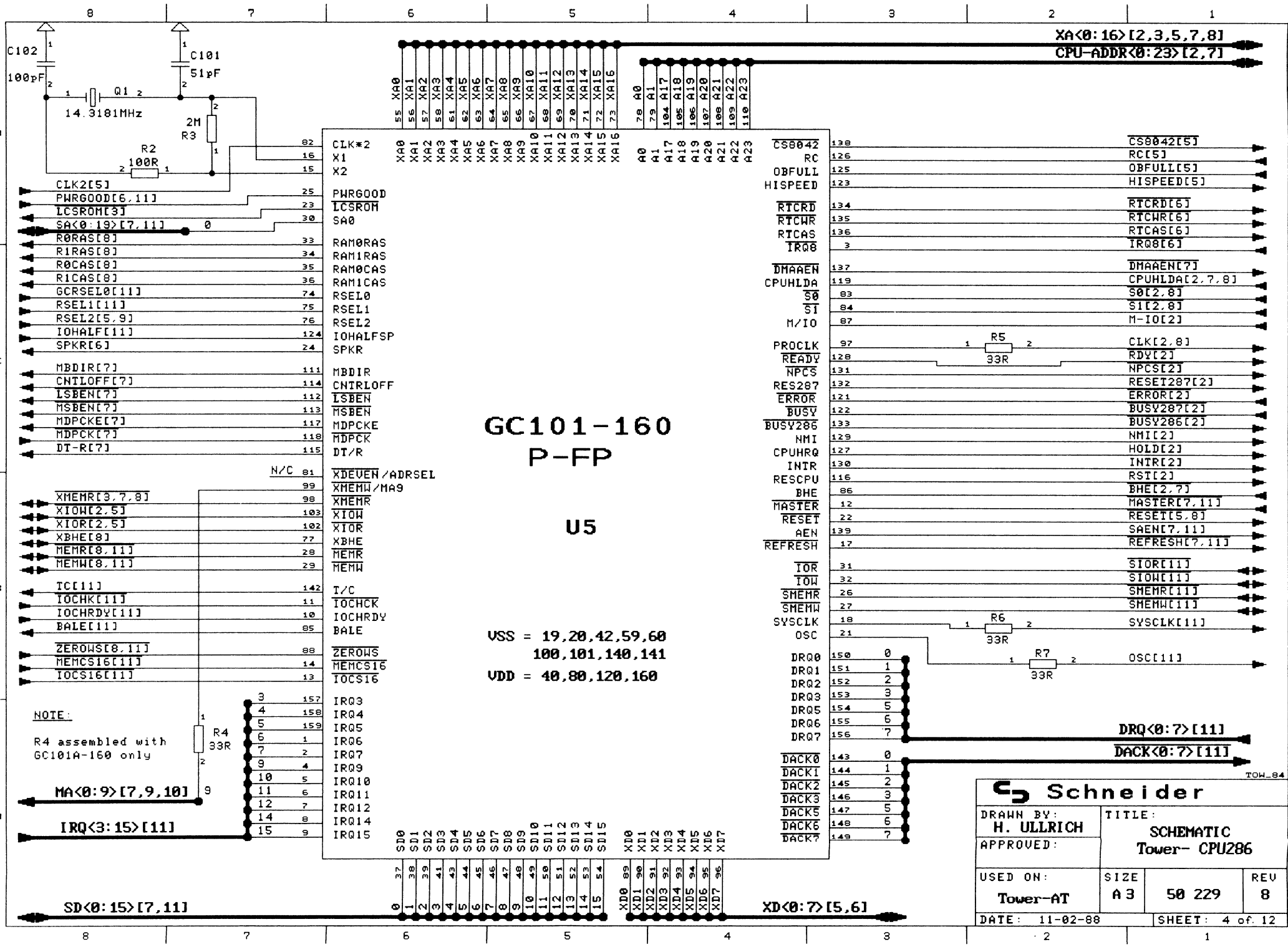

XA<0:23>[3,4,5,7,8]
RST[4]
BUSY286[4]
NMI[4]
INTR[4]
HOLD[4]
RDY[4]
NPCS[4]
RESET287[4]
80287
80286
U2
U1
RN1/2 10K
RN1/1 10K
R1 10K
R28 10K
R29 10K
C100 47nF
+5V
S0
S1
CPUHLDA[4,7,8]
M-IO[4]
S1[4,8]
S0[4,8]
BHE[4,7]
CA20[7]
CPU-ADDR<0:23>[4,7]
CPU-DATEN<0:15>[7]
CLK[4,8]
XIOW[4,5]
XIOR[4,5]
CLK287[5]
BUSY287[4]
ERROR[4]
VCC = 9
VSS=10,30
VCC = 30,62
VSS = 9,35,60
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC Tower- CPU286
USED ON: Tower-AT
SIZE A3
50 229
REV 8
DATE: 11-02-88
SHEET: 2 of 12
TOW_02

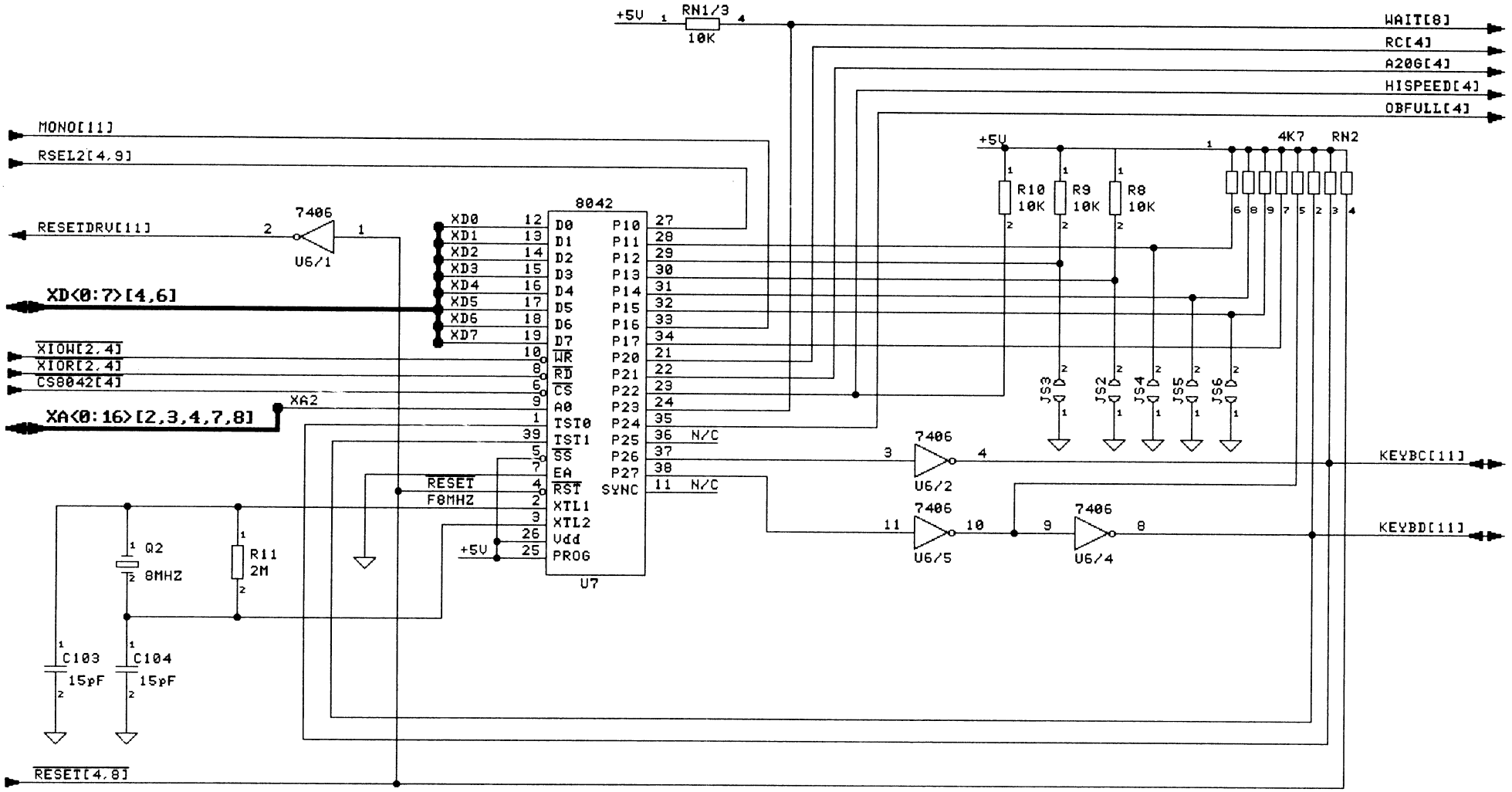


TOW_83

Schneider

DRAWN BY: B.ASSMANN	TITLE: SCHEMATIC Tower- CPU286		
APPROVED:			
USED ON: Tower-AT	SIZE A3	50 229	REV 8
DATE: 11-02-88	SHEET: 3 of 12		

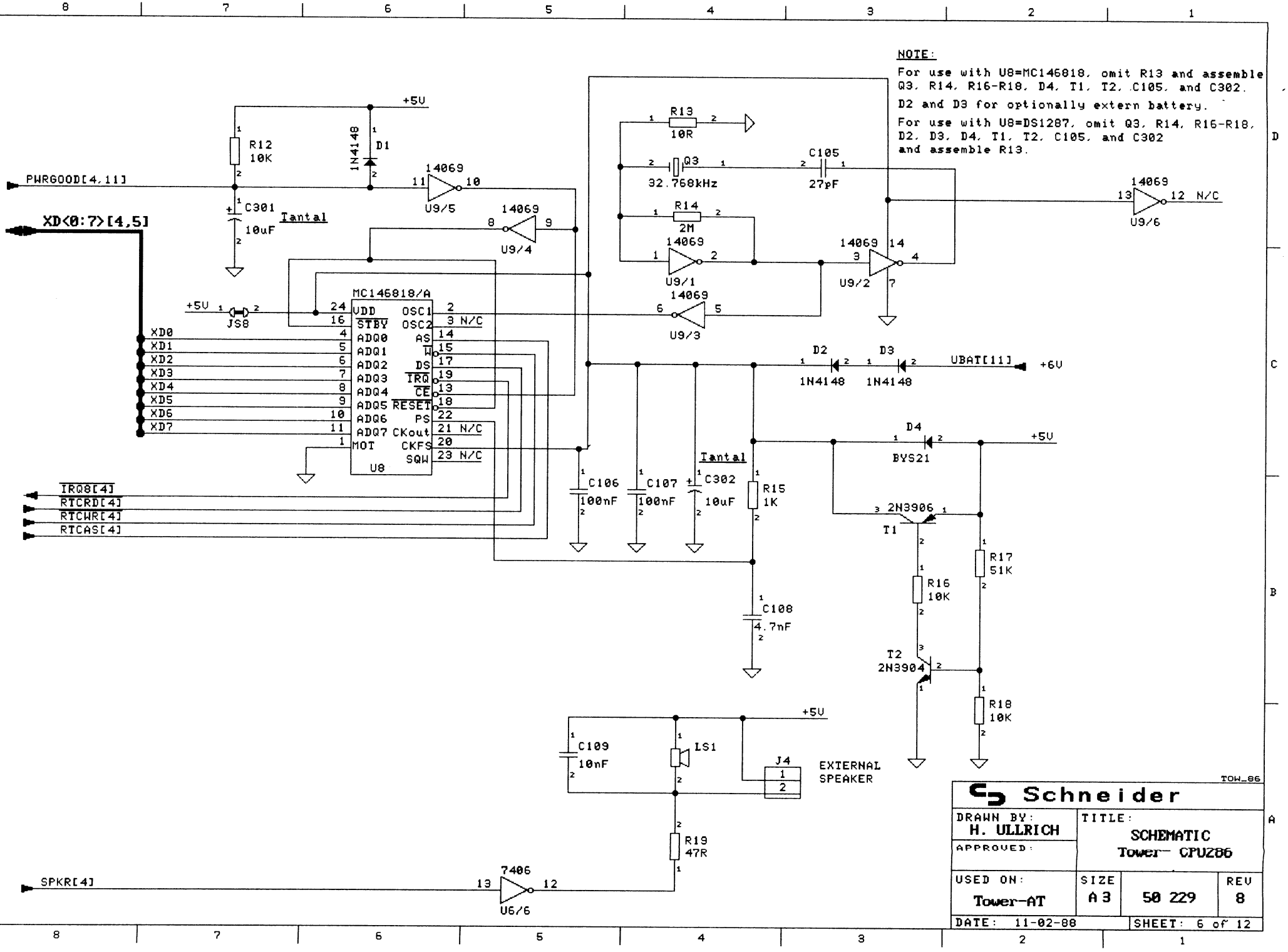

GC101-160
P-FP
U5
C102
100pF
C101
51pF
Q1
14.3181MHz
2M
R3
R2
100R
R5
33R
R6
33R
R7
33R
R4
33R
NOTE:
R4 assembled with
GC101A-160 only
VSS = 19,20,42,59,60
100,101,140,141
VDD = 40,80,120,160
XA<0:16>[2,3,5,7,8]
CPU-ADDR<0:23>[2,7]
CLK2[5]
PWRGOOD[6,11]
LCSROM[3]
SA<0:19>[7,11]
R0RAS[8]
R1RAS[8]
R0CAS[8]
R1CAS[8]
GCRSEL0[11]
RSEL1[11]
RSEL2[5,9]
IOHALF[11]
SPKR[6]
MBDIR[7]
CNTLOFF[7]
LSBEN[7]
MSBEN[7]
MDPCKE[7]
MDPCK[7]
DT-R[7]
XMEMR[3,7,8]
XIOW[2,5]
XIOR[2,5]
XBHE[8]
MEMR[8,11]
MEMW[8,11]
IC[11]
IOCHK[11]
IOCHRDY[11]
BALE[11]
ZEROWS[8,11]
MEMCS16[11]
IOCS16[11]
MA<0:9>[7,9,10]
IRQ<3:15>[11]
SD<0:15>[7,11]
XD<0:7>[5,6]
DRQ<0:7>[11]
DACK<0:7>[11]
CS8042[5]
RC[5]
OBFULL[5]
HISPEED[5]
RTCRD[6]
RTCWR[6]
RTCAS[6]
IRQ8[6]
DMAAEN[7]
CPUHLDA[2,7,8]
S0[2,8]
S1[2,8]
M-IO[2]
CLK[2,8]
RDY[2]
NPCS[2]
RESET287[2]
ERROR[2]
BUSY287[2]
BUSY286[2]
NMI[2]
HOLD[2]
INTR[2]
RSI[2]
BHE[2,7]
MASTER[7,11]
RESET[5,8]
SAEN[7,11]
REFRESH[7,11]
SIOR[11]
SIOW[11]
SMEMR[11]
SMEMW[11]
SYSCLK[11]
OSC[11]
TOW_84
Schneider
DRAWN BY: H. ULLRICH
APPROVED:
TITLE: SCHEMATIC Tower- CPU286
USED ON: Tower-AT
SIZE A3
50 229
REV 8
DATE: 11-02-88
SHEET: 4 of 12

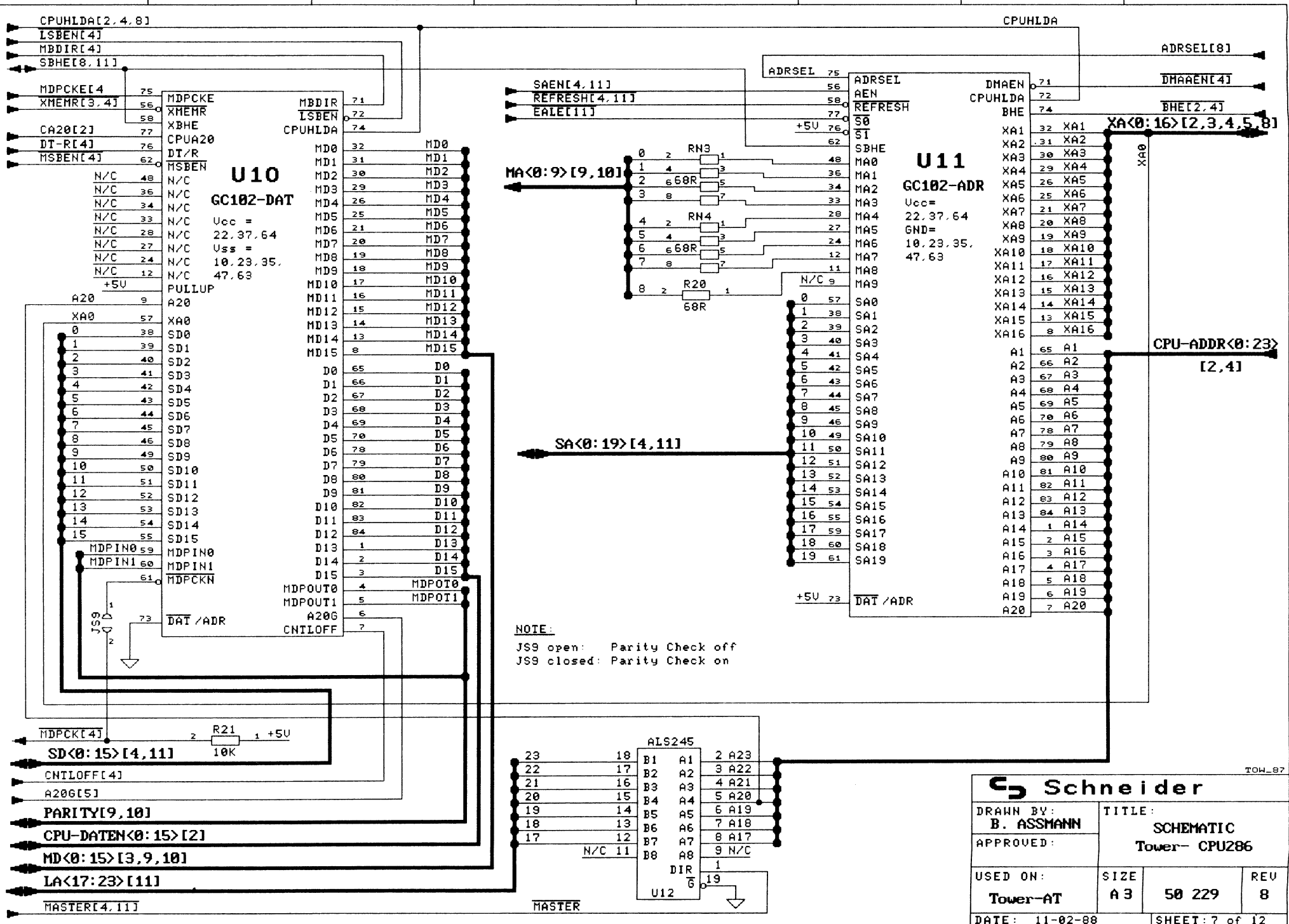


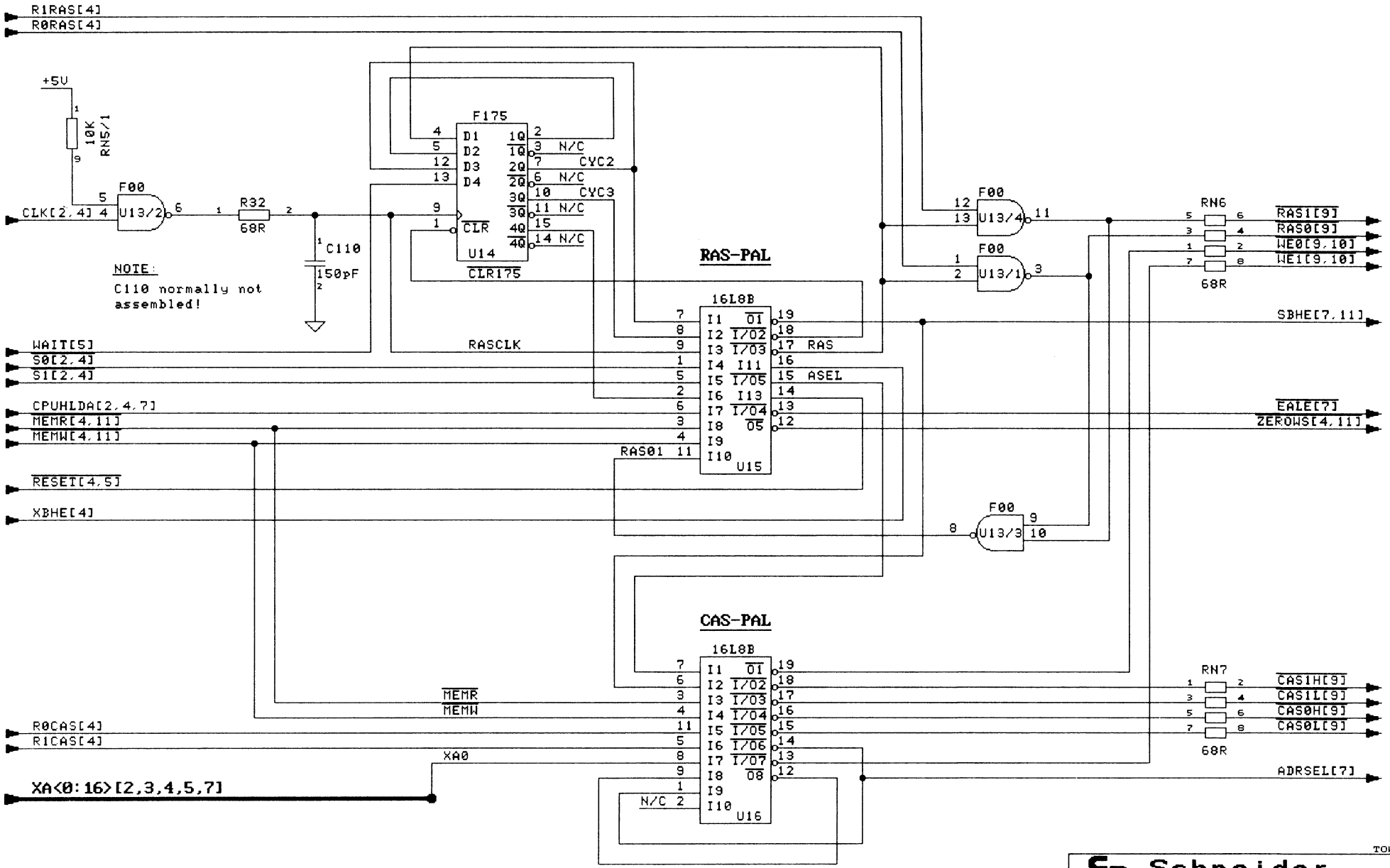
TOW_85

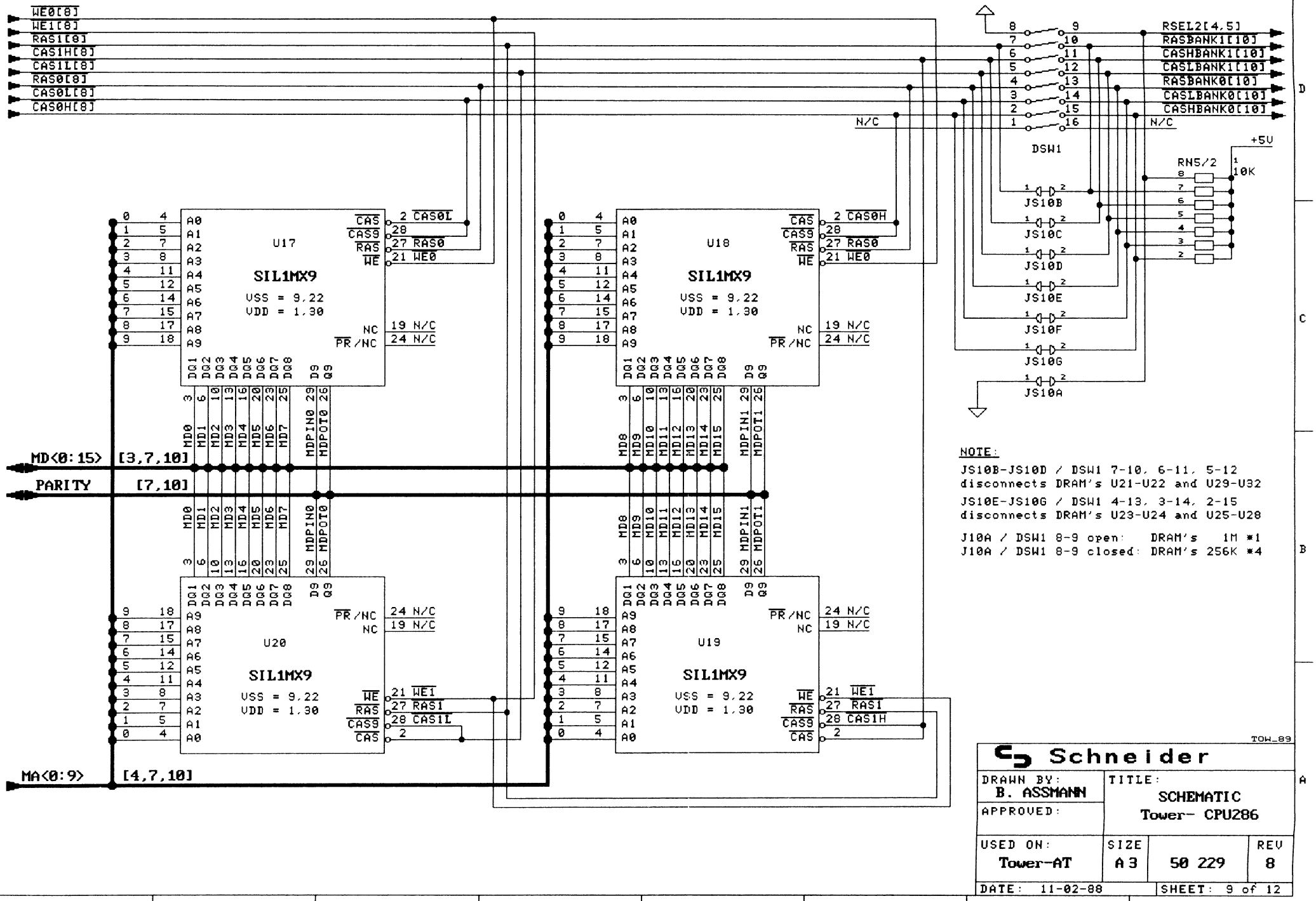
Schneider

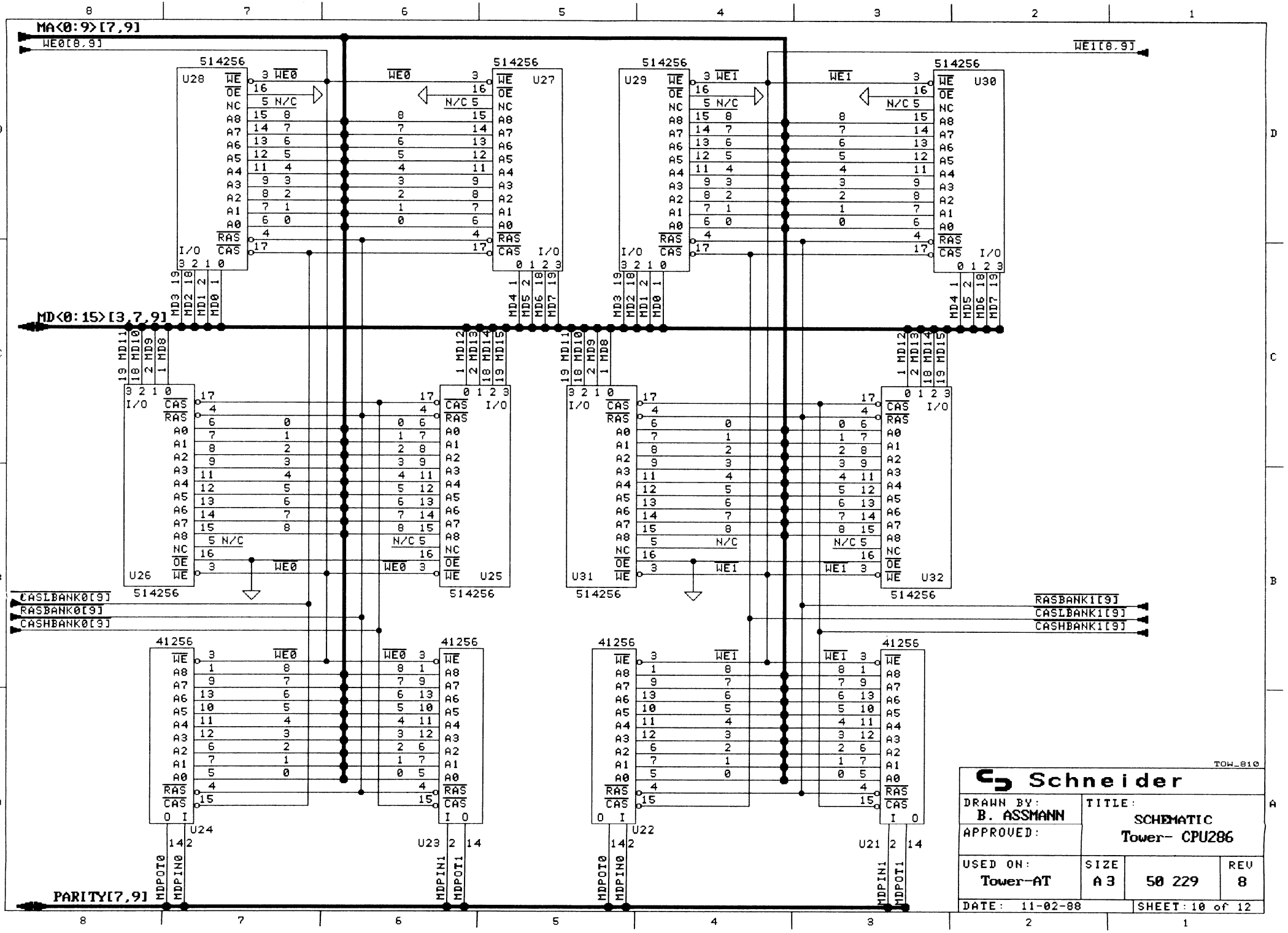
DRAWN BY: H.ULLRICH	TITLE: SCHEMATIC Tower- CPU286		
APPROVED:			
USED ON: Tower-AT	SIZE A3	50 229	REV 8
DATE: 11-02-88	SHEET: 5 of 12		

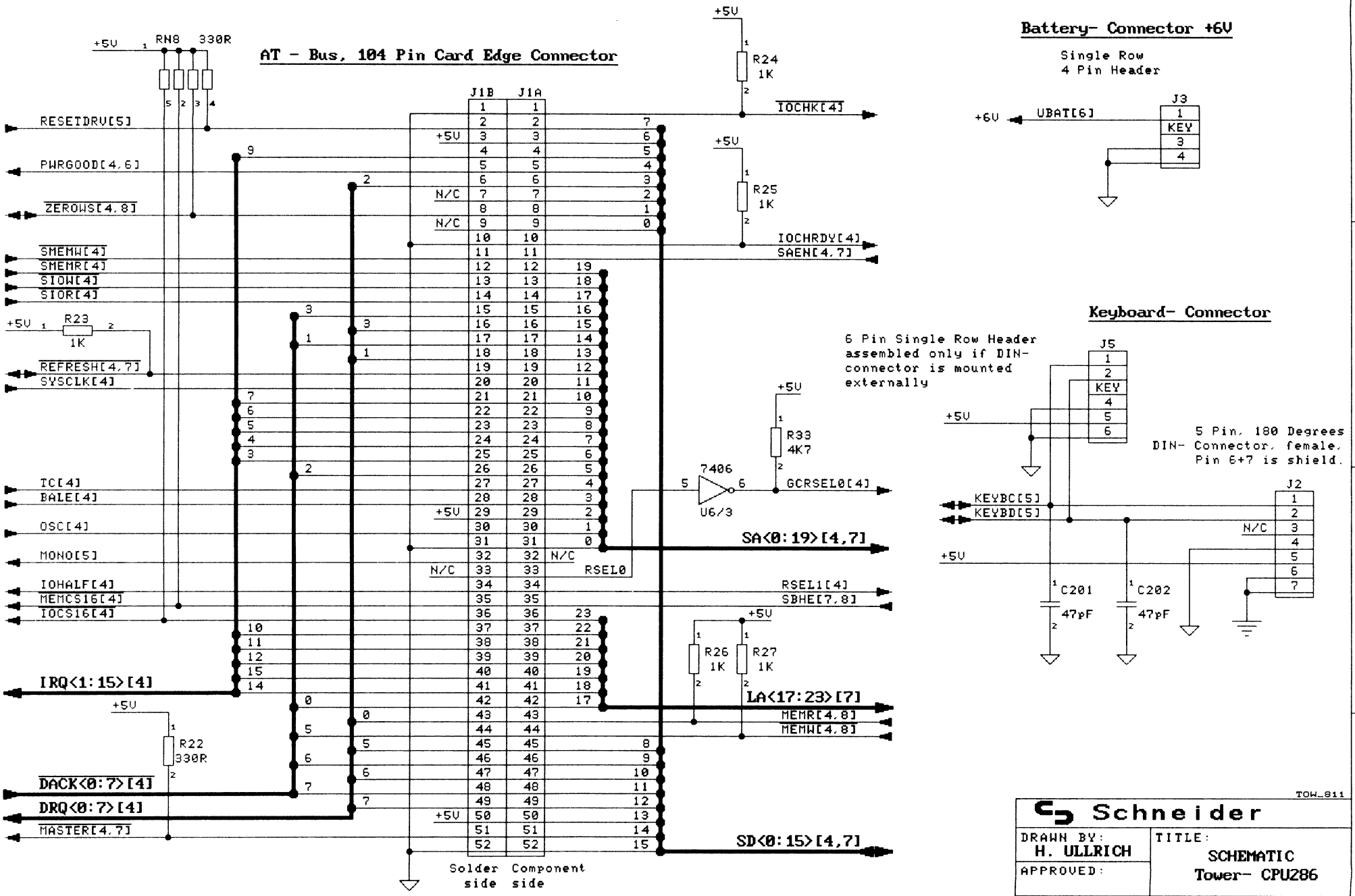

NOTE:
For use with U8=MC146818, omit R13 and assemble Q3, R14, R16-R18, D4, T1, T2, C105, and C302.
D2 and D3 for optionally extern battery.
For use with U8=DS1287, omit Q3, R14, R16-R18, D2, D3, D4, T1, T2, C105, and C302 and assemble R13.
+5U
R12
10K
1N4148
D1
PWRGOOD[4,11]
14069
U9/5
C301
10uF
Tantal
XD<0:7>[4,5]
14069
U9/4
MC146818/A
U8
VDD
STBY
ADQ0
ADQ1
ADQ2
ADQ3
ADQ4
ADQ5
ADQ6
ADQ7
MOT
OSC1
OSC2
AS
W
DS
IRQ
CE
RESET
PS
CKout
CKFS
SQW
N/C
JS8
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
IRQ8[4]
RTCRD[4]
RTCWR[4]
RTCAS[4]
R13
10R
Q3
32.768kHz
C105
27pF
R14
2M
14069
U9/1
14069
U9/2
14069
U9/3
14069
U9/6
N/C
D2
D3
1N4148
1N4148
UBAT[11]
+6U
D4
BYS21
C106
100nF
C107
100nF
C302
10uF
Tantal
R15
1K
C108
4.7nF
2N3906
T1
R17
51K
R16
10K
T2
2N3904
R18
10K
C109
10nF
LS1
J4
EXTERNAL
SPEAKER
R19
47R
SPKR[4]
7406
U6/6
TOW_86
Schneider
DRAWN BY:
H. ULLRICH
APPROVED:
TITLE:
SCHEMATIC
Tower- CPU286
USED ON:
Tower-AT
SIZE
A3
50 229
REV
8
DATE: 11-02-88
SHEET: 6 of 12


CPUHLDA[2,4,8]
LSBEN[4]
MBDIR[4]
SBHE[8,11]
MDPCKE[4]
XMEMR[3,4]
CA20[2]
DT-R[4]
MSBEN[4]
U10
GC102-DAT
Vcc = 22,37,64
Vss = 10,23,35,47,63
MDPCKE
XMEMR
XBHE
CPUA20
DT/R
MSBEN
PULLUP
A20
XA0
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
MDPIN0
MDPIN1
MDPCKN
DAT/ADR
MBDIR
LSBEN
CPUHLDA
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
MDPOUT0
MDPOUT1
A20G
CNTLOFF
JS9
MDPCK[4]
R21
10K
+5V
SD<0:15>[4,11]
CNTLOFF[4]
A20G[5]
PARITY[9,10]
CPU-DATEN<0:15>[2]
MD<0:15>[3,9,10]
LA<17:23>[11]
MASTER[4,11]
SAEN[4,11]
REFRESH[4,11]
EALE[11]
MA<0:9>[9,10]
RN3
RN4
68R
R20
68R
SA<0:19>[4,11]
U11
GC102-ADR
Vcc= 22,37,64
GND= 10,23,35,47,63
ADRSEL
AEN
REFRESH
S0
S1
SBHE
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
DAT/ADR
DMAEN
CPUHLDA
BHE
XA1
XA2
XA3
XA4
XA5
XA6
XA7
XA8
XA9
XA10
XA11
XA12
XA13
XA14
XA15
XA16
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
ADRSEL[8]
DMAAEN[4]
BHE[2,4]
XA<0:16>[2,3,4,5,8]
CPU-ADDR<0:23>[2,4]
ALS245
U12
DIR
G
MASTER
NOTE:
JS9 open: Parity Check off
JS9 closed: Parity Check on
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC Tower- CPU286
USED ON: Tower-AT
SIZE A3
50 229
REV 8
DATE: 11-02-88
SHEET: 7 of 12
TOW_87


R1RAS[4]
R0RAS[4]
+5V
10K
RN5/1
F00
U13/2
CLK[2,4] 4
R32
68R
C110
150pF
NOTE:
C110 normally not assembled!
F175
U14
CLR175
CYC2
CYC3
N/C
RAS-PAL
16L8B
U15
RASCLK
RAS
ASEL
RAS01
WAIT[5]
S0[2,4]
S1[2,4]
CPUHLDA[2,4,7]
MEMR[4,11]
MEMW[4,11]
RESET[4,5]
XBHE[4]
U13/4
U13/1
U13/3
RN6
RAS1[9]
RAS0[9]
WE0[9,10]
WE1[9,10]
68R
SBHE[7,11]
EALE[7]
ZEROWS[4,11]
CAS-PAL
U16
MEMR
MEMW
R0CAS[4]
R1CAS[4]
XA0
XA<0:16>[2,3,4,5,7]
RN7
CAS1H[9]
CAS1L[9]
CAS0H[9]
CAS0L[9]
ADRSEL[7]
TOW_88
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC TOWER CPU 80Z86
USED ON: TOWER-AT
SIZE A3
50 229
REV 8
DATE: 11-02-88
SHEET: 8 of 12

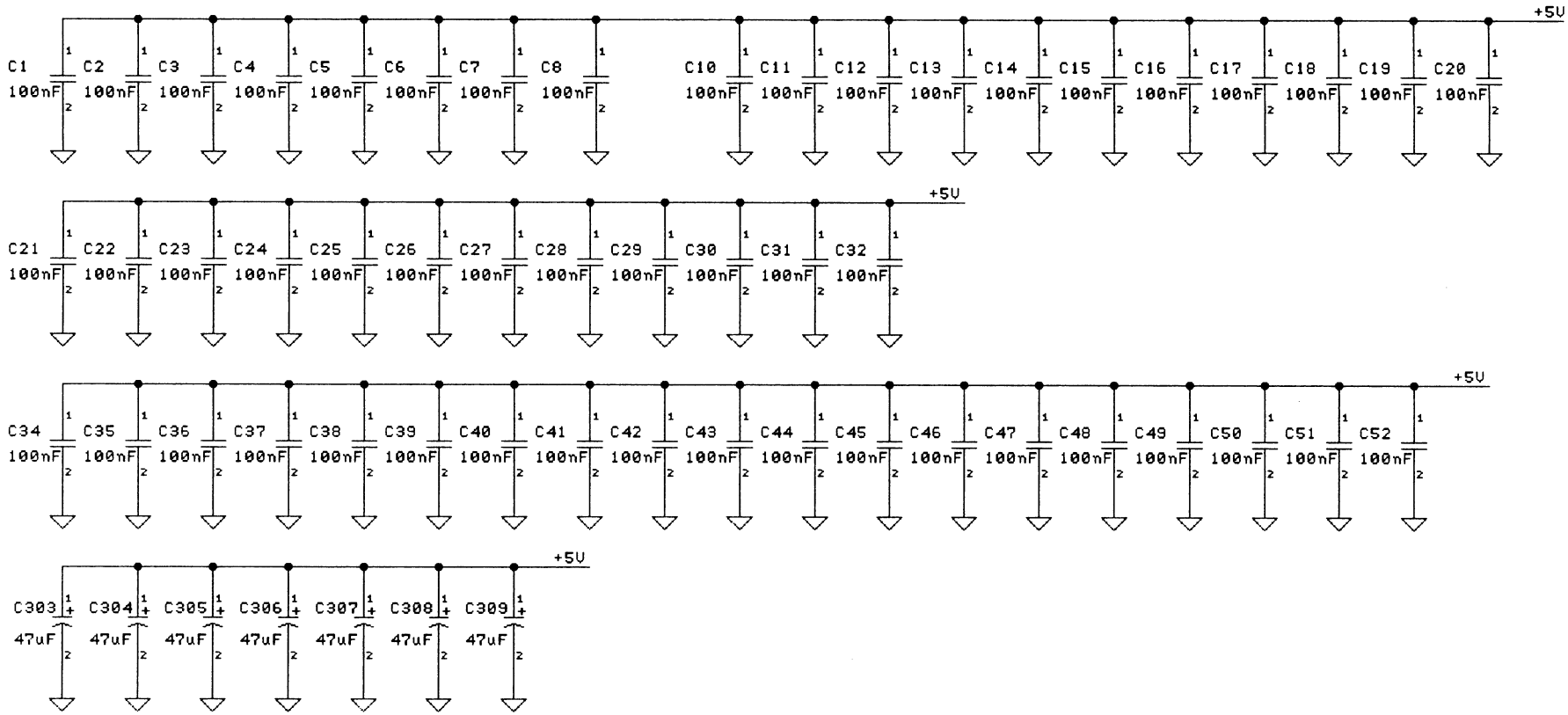

WE0[8]
WE1[8]
RAS1[8]
CAS1H[8]
CAS1L[8]
RAS0[8]
CAS0L[8]
CAS0H[8]
N/C
RSEL2[4,5]
RASBANK1[10]
CASHBANK1[10]
CASLBANK1[10]
RASBANK0[10]
CASLBANK0[10]
CASHBANK0[10]
N/C
DSW1
+5V
RN5/2
10K
JS10B
JS10C
JS10D
JS10E
JS10F
JS10G
JS10A
U17
U18
U19
U20
SIL1MX9
VSS = 9.22
VDD = 1.30
MD<0:15> [3,7,10]
PARITY [7,10]
MA<0:9> [4,7,10]
NOTE:
JS10B-JS10D / DSW1 7-10, 6-11, 5-12
disconnects DRAM's U21-U22 and U29-U32
JS10E-JS10G / DSW1 4-13, 3-14, 2-15
disconnects DRAM's U23-U24 and U25-U28
J10A / DSW1 8-9 open: DRAM's 1M *1
J10A / DSW1 8-9 closed: DRAM's 256K *4
TOW_89
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC Tower- CPU286
USED ON: Tower-AT
SIZE A3
50 229
REV 8
DATE: 11-02-88
SHEET: 9 of 12


MA<0:9>[7,9]
WE0[8,9]
WE1[8,9]
MD<0:15>[3,7,9]
514256
U28
U27
U29
U30
U26
U25
U31
U32
41256
U24
U23
U22
U21
CASLBANK0[9]
RASBANK0[9]
CASHBANK0[9]
RASBANK1[9]
CASLBANK1[9]
CASHBANK1[9]
PARITY[7,9]
MDPOT0
MDPIN0
MDPIN1
MDPOT1
TOW_810
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC Tower- CPU286
USED ON: Tower-AT
SIZE A3
50 229
REV 8
DATE: 11-02-88
SHEET: 10 of 12



TOW_811

Schneider			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC Tower- CPUZ86		
APPROVED:			
USED ON: Tower-AT	SIZE A3	50 229	REV 8
DATE: 11-02-88	SHEET: 11 of 12		



TOW_812

Schneider

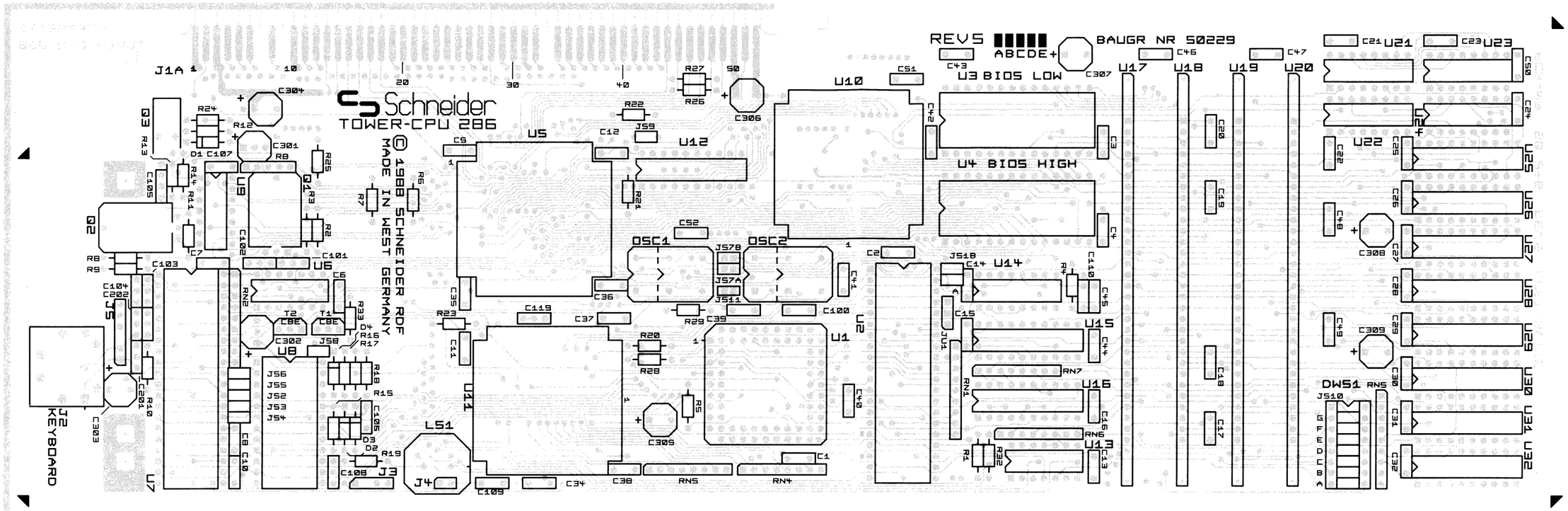
DRAWN BY: B. ASSMANN	TITLE: SCHEMATIC Tower- CPU286
APPROVED:	
USED ON: Tower-AT	SIZE A3 | 50 229 | REV 8
DATE: 11-02-88	SHEET: 12 of 12

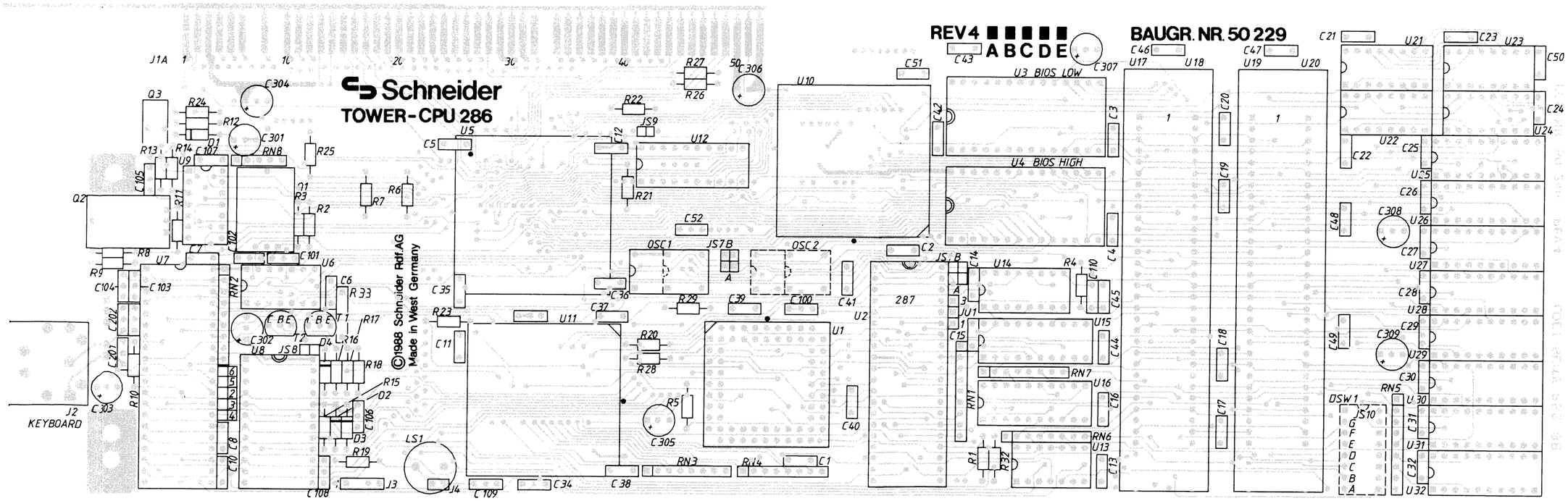
Ersatzteilliste für Platine Best. (D) Tower AT CPU
Parts List PCB (D) Tower AT CPU

Bestell-Nr. Part.-No.	Bezeichnung	Description	Zeich.-Pos. Ref.-No.	Preisgruppe
50 115 00	IC 80286	IC 80286	U 1	F 4
50 444 00	IC EPROM 256K prog.	IC EPROM 256K prog.	U 3	C 9
50 445 00	IC EPROM 256K prog.	IC EPROM 256K prog.	U 4	C 9
50 047 00	IC GC 101C CPU Contr. (Rev. 4)	IC GC 101C CPU Contr. (Rev. 4)	U 5	F 5
50 776 00	IC GC 101D CPU Contr. (Rev. 5)	IC GC 101D CPU Contr. (Rev. 5)	U 5	F 5
50 122 00	IC 7406	IC 7406	U 6	A 7
50 243 00	IC 8042 prog.	IC 8042 prog.	U 7	C 3
50 177 00	IC DS 1287	IC DS 1287	U 8	D 4
50 323 00	IC MC 14069	IC MC 14069	U 9	A 3
50 045 00	IC GC 102 Data	IC GC 102 Data	U 10	D 7
50 046 00	IC GC 102A Address	IC GC 102A Address	U 11	D 7
50 249 00	IC 74 ALS 245	IC 74 ALS 245	U 12	B 1
50 123 00	IC 74 F 00	IC 74 F 00	U 13	A 3
50 242 00	IC 74 F 175	IC 74 F 175	U 14	A 8
50 334 00	IC PAL 16L8BCN RAS-PAL	IC PAL 16L8BCN RAS-PAL	U 15	B 8
50 333 00	IC PAL 16L8BCN CAS-PAL	IC PAL 16L8BCN CAS-PAL	U 16	B 8
50 160 00	IC DRAM 256×4	IC DRAM 256×4	U 25-28	F 4
50 379 00	IC 74 HC 132	IC 74 HC 132	U 33	A 5
50 338 00	Diode 1 N 4148	Diode 1 N 4148	D 1,5	A 0
50 325 00	Quarz 14,31818 MHz	Quarz 14.31818 MHz	Q 1	B 3
50 326 00	Quarz 8,0 MHz	Quarz 8.0 MHz	Q 2	B 0
50 327 00	Osz. 20,0 MHz	Osc. 20.0 MHz	OSC 1	C 0
50 345 00	Elko rad. 47µF/16V	CE 47µF/16V	C 303-309	A 2
50 344 00	Tantal 10µF/16V	CE 10µF/16V	C 301	A 4
50 381 00	Tantal 1µF/16V	CE 1µF/16V	C 310	A 3
50 316 00	R-Netzwerk 8×10K	Network 8×10K	RN 1,5	A 3
50 319 00	R-Netzwerk 8×4K7	Network 8×4K7	RN 2	A 3
50 382 00	R-Netzwerk 4×68R	Network 4×68R	RN 3, 4, 6, 7	A 2
50 331 00	R-Netzwerk 4×330R	Network 4×330R	RN 8	A 2
50 332 00	Summer	Buzzer	LS 1	A 8
50 181 00	Buchse Dioden 5 Pin	Socket Diode 5 Pin	J 2	A 5

CPU

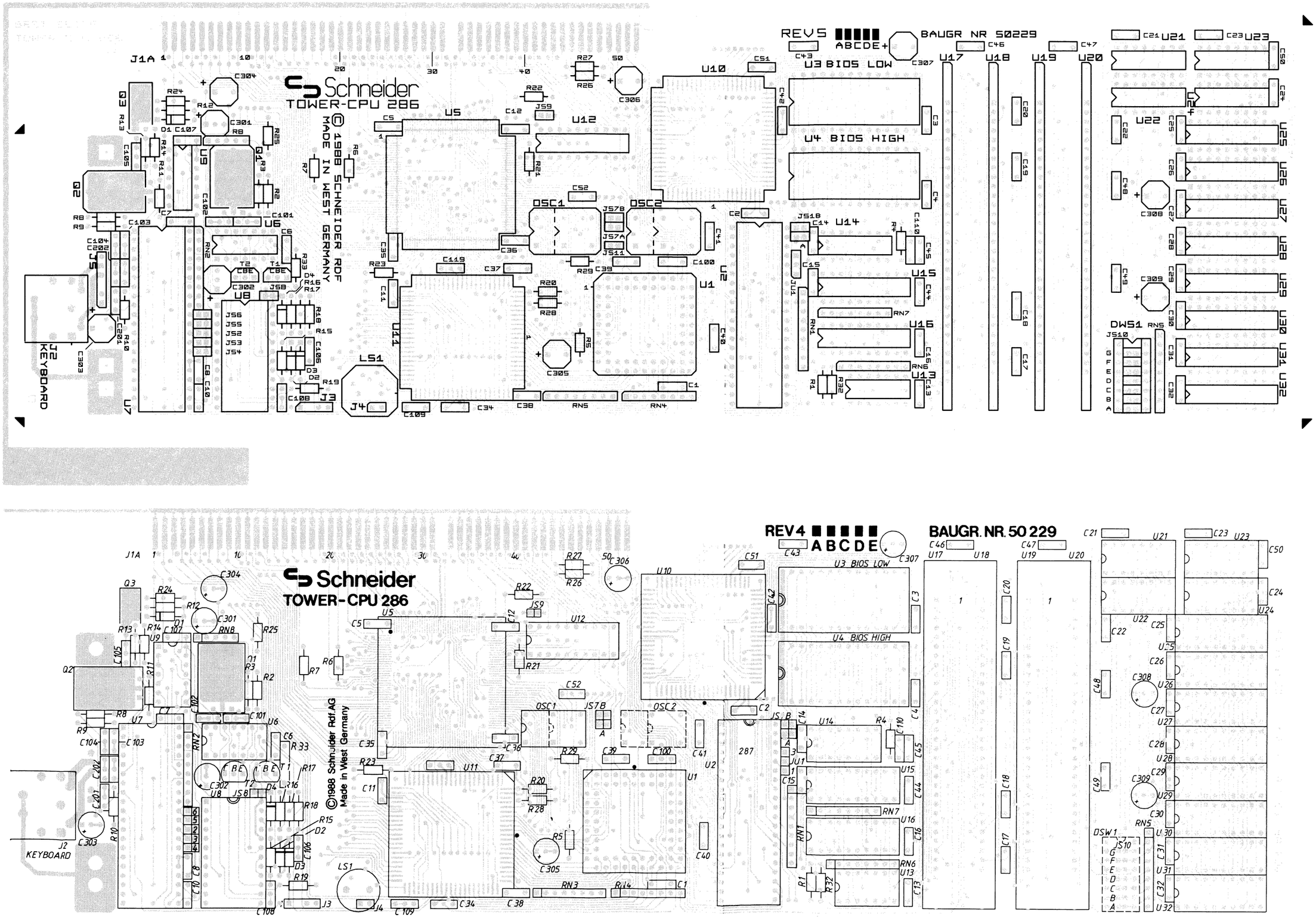
Soldering side





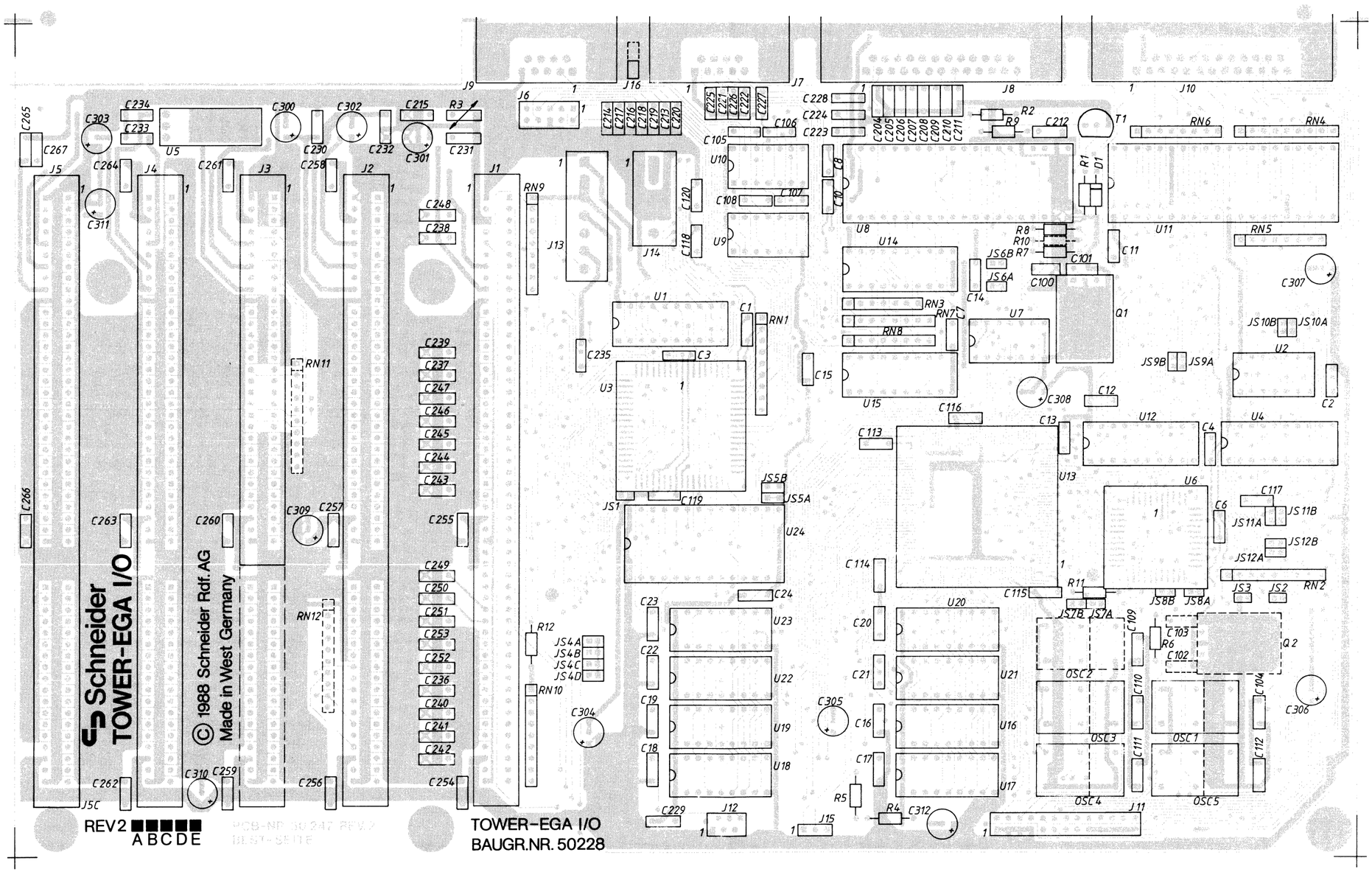
CPU

Component side



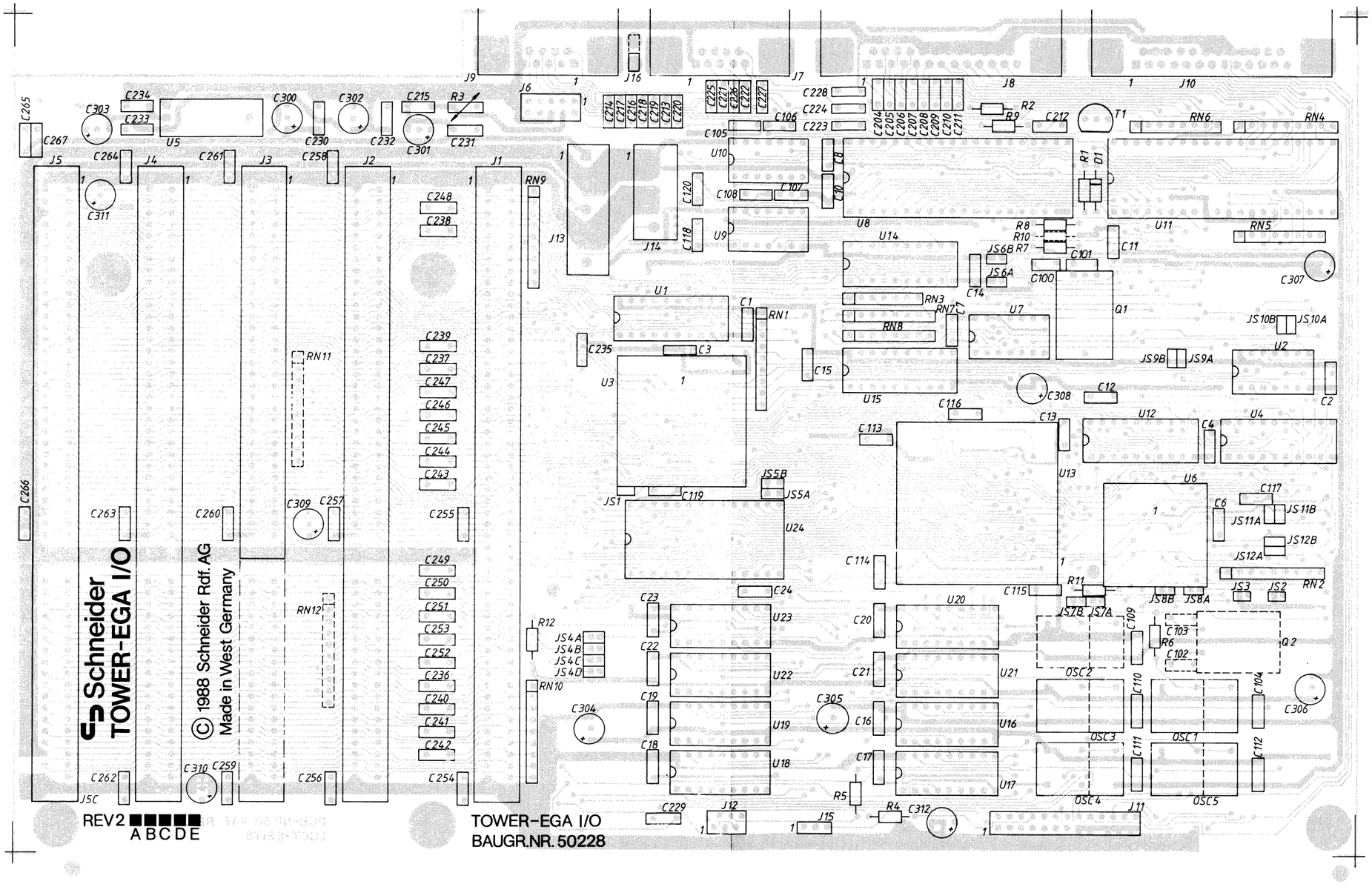
EGA I/0

Component side



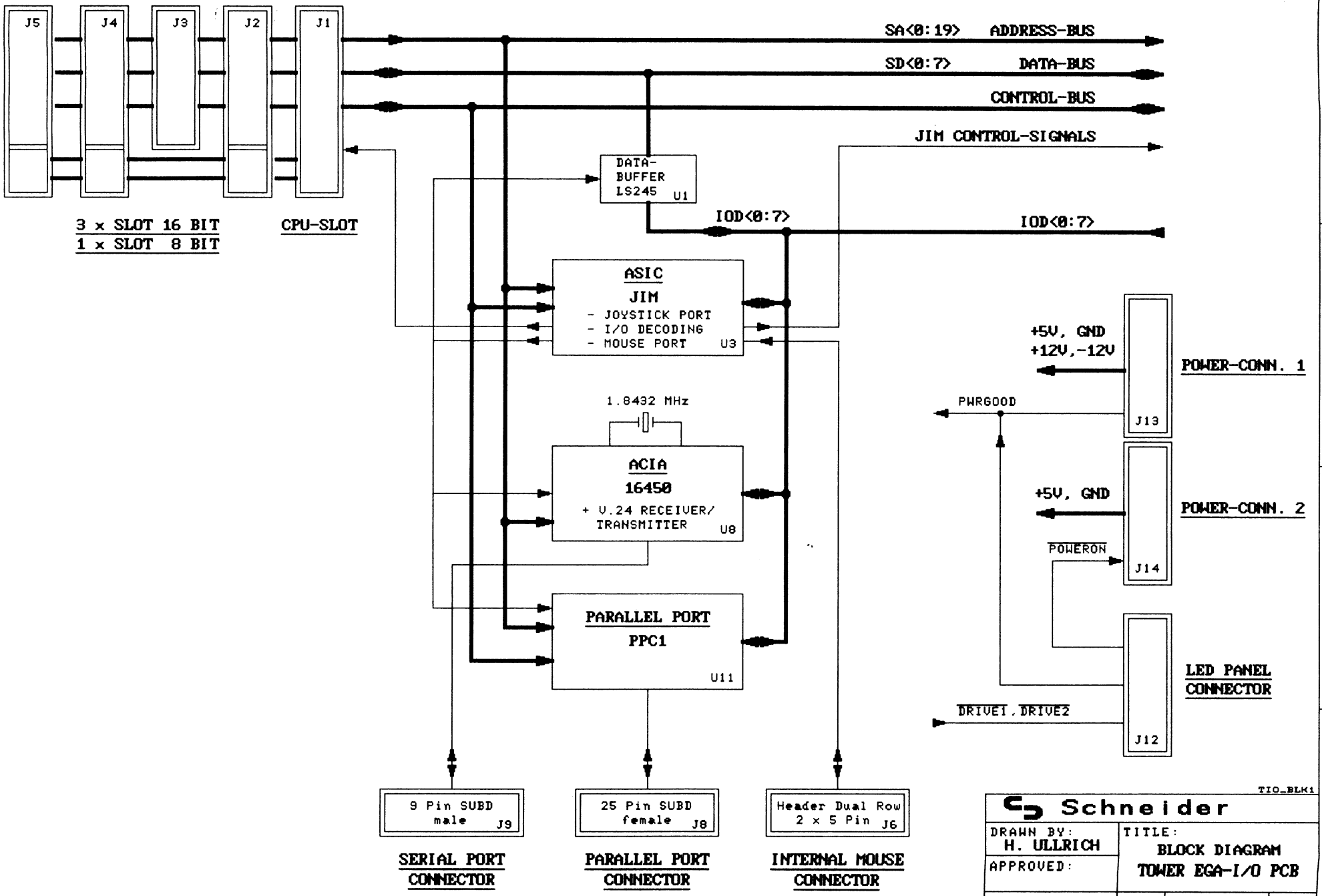
EGA I/0

Soldering side



Ersatzteilliste für Platine Best. (D) Tower EGA I/O
Parts List P.C.B (D) Tower EGA I/O

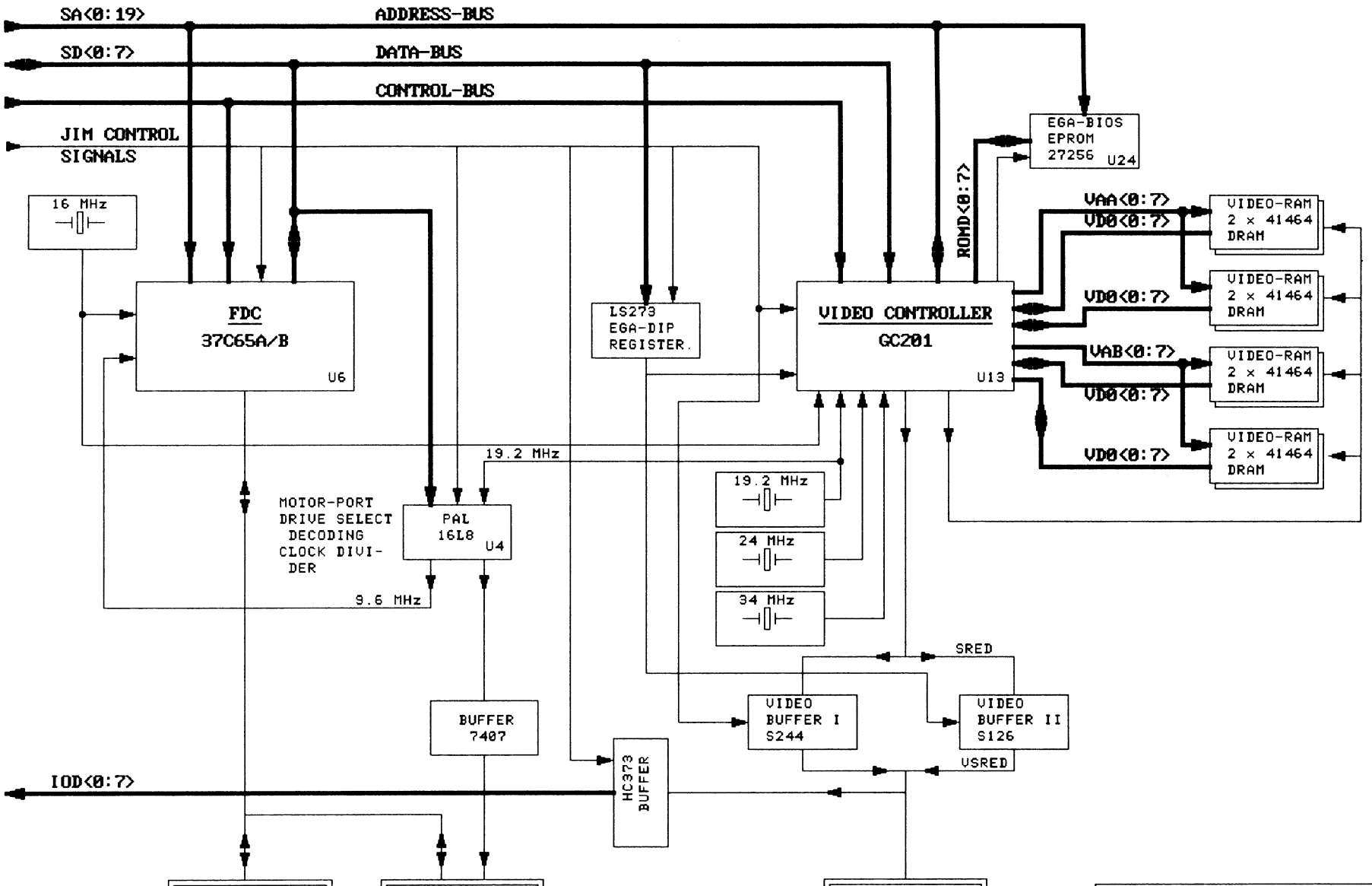
Bestell-Nr. Part.-No.	Bezeichnung	Description	Zeich.-Pos. Ref.-No.	Preisgruppe
50 129 00	IC 74LS245	IC 74LS245	U 1	A 7
50 237 00	IC 7407	IC 7407	U 2	A 8
50 101 00	IC JIM TC17 GO 22AT	IC JIM TC17 GO 22AT	U 3	C 7
50 311 00	IC PAL 16 L8A Peog.	IC PAL 16 L8A Prog.	U 4	B 4
50 238 00	IC 7905 (TO220)	IC 7905 (TO220)	U 5	A 6
50 105 00	IC WD 37 C65A-JM00	IC WD 37 C65A-JM00	U 6	D 5
50 240 00	IC 74 F 126	IC 74 F 126	U 7	A 9
50 169 00	IC 16 C 450 PC	IC 16 C 450 PC	U 8	C 9
50 120 00	IC MC 1488	IC MC 1488	U 9	A 4
50 121 00	IC MC 1489	IC MC 1489	U 10	A 4
50 106 00	IC PPC 1	IC PPC 1	U 11	C 2
50 239 00	IC 74 LS 237	IC 74 LS 237	U 12	A 6
50 147 00	IC GC-201	IC GC-201	U 13	F 2
50 125 00	IC 74 HC 373	IC 74 HC 373	U 14	A 8
50 241 00	IC 74 F 244	IC 74 F 244	U 15	B 0
50 110 00	IC DRAM 64K×4 120ns	IC DRAM 64K×4 120ns	U 16-23	D 4
50 447 00	IC EPROM 256K prog.	IC EPROM 256K prog.	U 24	C 9
50 338 00	Diode 1 N 4148	Diode 1 N 4148	D 1	A 0
50 358 00	Trans BC 337 B	Trans BC 337 B	T 1	A 2
50 312 00	Quarz 1,8432 MHz	Quarz 1.8432 MHz	Q 1	B 6
50 313 00	Osz. 16,0 MHz	Osc. 16.0 MHz	OSC 1	C 0
50 337 00	Osz. 34,0 MHz	Osc. 34.0 MHz	OSC 3	C 0
50 315 00	Osz. 24,0 MHz	Osc. 24.0 MHz	OSC 4	C 0
50 314 00	Osz. 19,2 MHz	Osc. 19.2MHz	OSC 5	C 0
50 365 00	Elko rad. 10µF/25V	CE 10µF/25V	C 300-303	A 2
50 345 00	Elko rad. 47µF/16V	CE 47µF/16V	C 304-312	A 2
50 316 00	R-Netzwerk 8×10K	R-Network 8×10K	RN 1	A 3
50 317 00	R-Netzwerk 8×1K	R-Network 8×1K	RN 2	A 3
50 320 00	R-Netzwerk 6×680K	R-Network 6×680K	RN 3	A 2
50 319 00	R-Netzwerk 8×4K7	R-Network 8×4K7	RN 4, 9, 10	A 3
50 318 00	R-Netzwerk 4×33R	R-Network 4×33R	RN 5-8	A 2
50 372 00	R-Netzwerk 9×10K	R-Network 9×10K	RN 11, 12	A 2
50 321 00	Widerstand PTC 0R75	Resistor PTC 0R75	R 3	B 0
50 178 00	Buchse Cardedge 104 Pin	Socket Cardedge 104 Pin	J 1	B 5
50 179 00	Buchse Cardedge 98 Pin	Socket Cardedge 98 Pin	J 2, 4, 5	B 3
50 180 00	Buchse Cardedge 62 Pin	Socket Cardedge 62 Pin	J 3	B 1
50 252 00	Stiftleiste RM 2,54 10pol.	Connector RM 2.54 10-pol.	J 6	A 2
50 132 00	Buchse SUB D 9 Pin	Socket SUB D 9 Pin	J 7	A 9
50 133 00	Buchse SUB D 25 Pin	Socket SUB D 25 Pin	J 8, 10	B 2
50 131 00	Buchse SUB D 9 Pin	Socket SUB D 9 Pin	J 9	A 9
50 139 00	Stiftleiste RM 2,54 26pol.	Connector RM 2.54 26-pol.	J 11	A 4



TIO_BLK1

Schneider

DRAWN BY: H. ULLRICH	TITLE: BLOCK DIAGRAM TOWER EGA-I/O PCB		
APPROVED:			
USED ON: TOWER AT	SIZE A3	50 228	REV 2
DATE: 09-29-88	SHEET: 1 of 2		



TIO_BLK2

Schneider

DRAWN BY: H. ULLRICH	TITLE: BLOCK DIAGRAM TOWER EGA-I/O PCB		
APPROVED:			
USED ON: TOWER AT	SIZE A3	50 228	REV . 2
DATE: 09-29-88	SHEET: 2 of 2		

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
1	ADVANCED ENGINEERING RELEASE	04-27-88	RME
2	UPDATE	05-04-88	RME
3	UPDATE	05-24-88	RME
4	UPDATE, CORRECTIONS, ADDED BLOCK CAPS	06-22-88	H.ULLRICH
5	NEW LAYOUT (PCB REV.2)	07-11-88	RME
6	CHANGED 2 SIGNAL NAMES, ADDED PAGE REFERENCES	08-10-88	H.ULLRICH
7	CHANGED R8 VALUE TO 1K, ADDED C268 (C268 IS NOT INCLUDED IN THE LAYOUT OR SILKSCREEN BUT AN ADDON REWORK!)	09-15-88	H.ULLRICH
8	ADDED C121 (NOT INCLUDED IN LAYOYT OR SILKSCREEN - ADD-ON REWORK!) BUG FIX FOR VC-001 VIDEO CHIP	11-18-88	B.ASSMANN

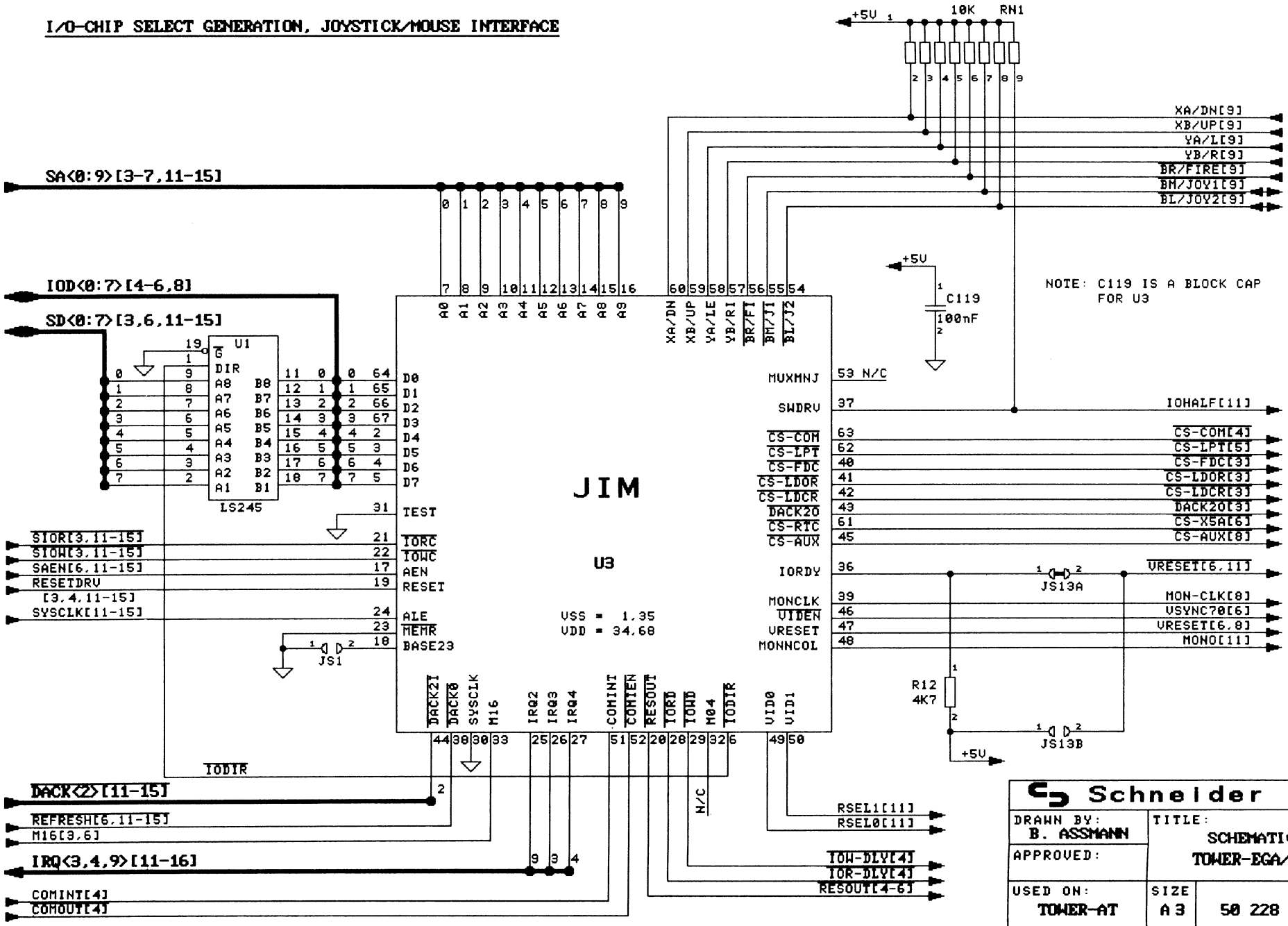
DRAWING FILES:	CONTENTS:
TIO_81.DWG	THIS SHEET
TIO_82.DWG	ASIC JIM
TIO_83.DWG	FLOPPY INTERFACE
TIO_84.DWG	SERIAL INTERFACE
TIO_85.DWG	PARALLEL INTERFACE
TIO_86.DWG	VIDEO CONTROLLER
TIO_87.DWG	VIDEO RAM, CHAR. ROM
TIO_88.DWG	VIDEO INTERFACE
TIO_89.DWG	CONNECTORS I
TIO_810.DWG	CONNECTORS II
TIO_811.DWG	CPU SLOT
TIO_812.DWG	NORMAL SLOT
TIO_813.DWG	NORMAL SLOT
TIO_814.DWG	NORMAL SLOT
TIO_815.DWG	NORMAL SLOT
TIO_816.DWG	BLOCK CAPS, SPARE GATES

TIO_81

Schneider

DRAWN BY: B. ASSMANN	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88		SHEET: 1 of 16	

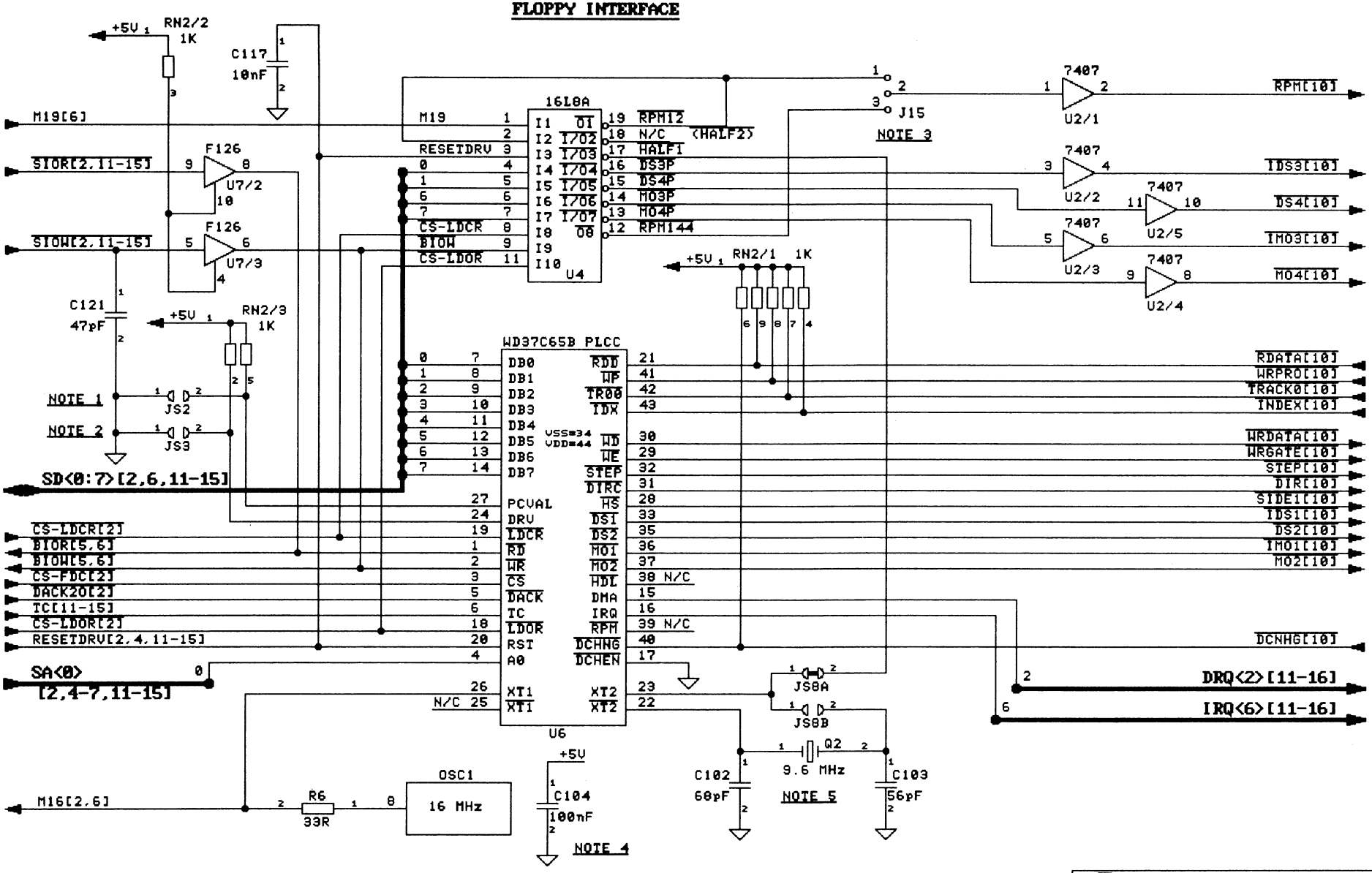
I/O-CHIP SELECT GENERATION, JOYSTICK/MOUSE INTERFACE



Schneider			
DRAWN BY: B. ASSMANN	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 2 of 16		

TIO_82

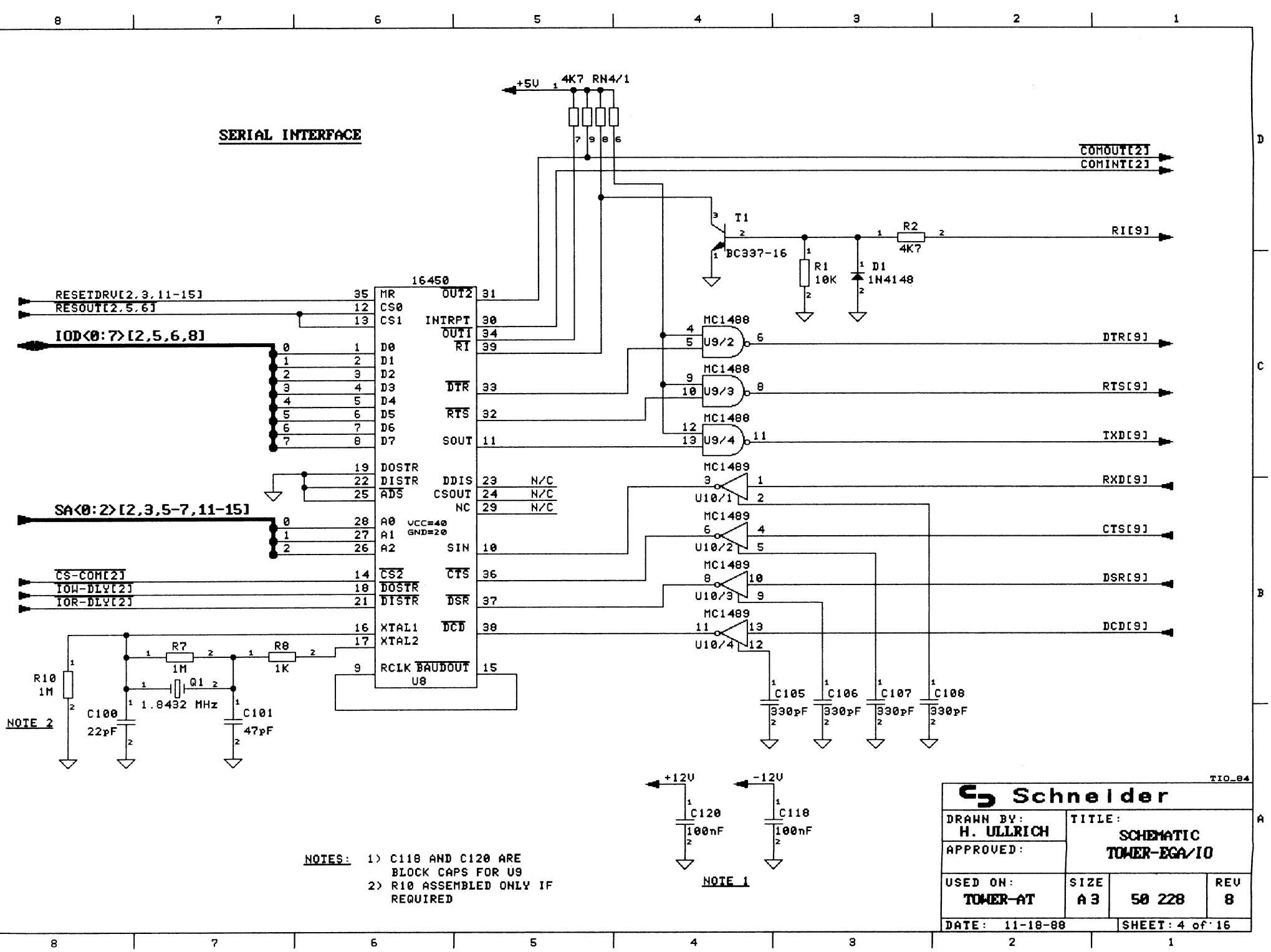
FLOPPY INTERFACE



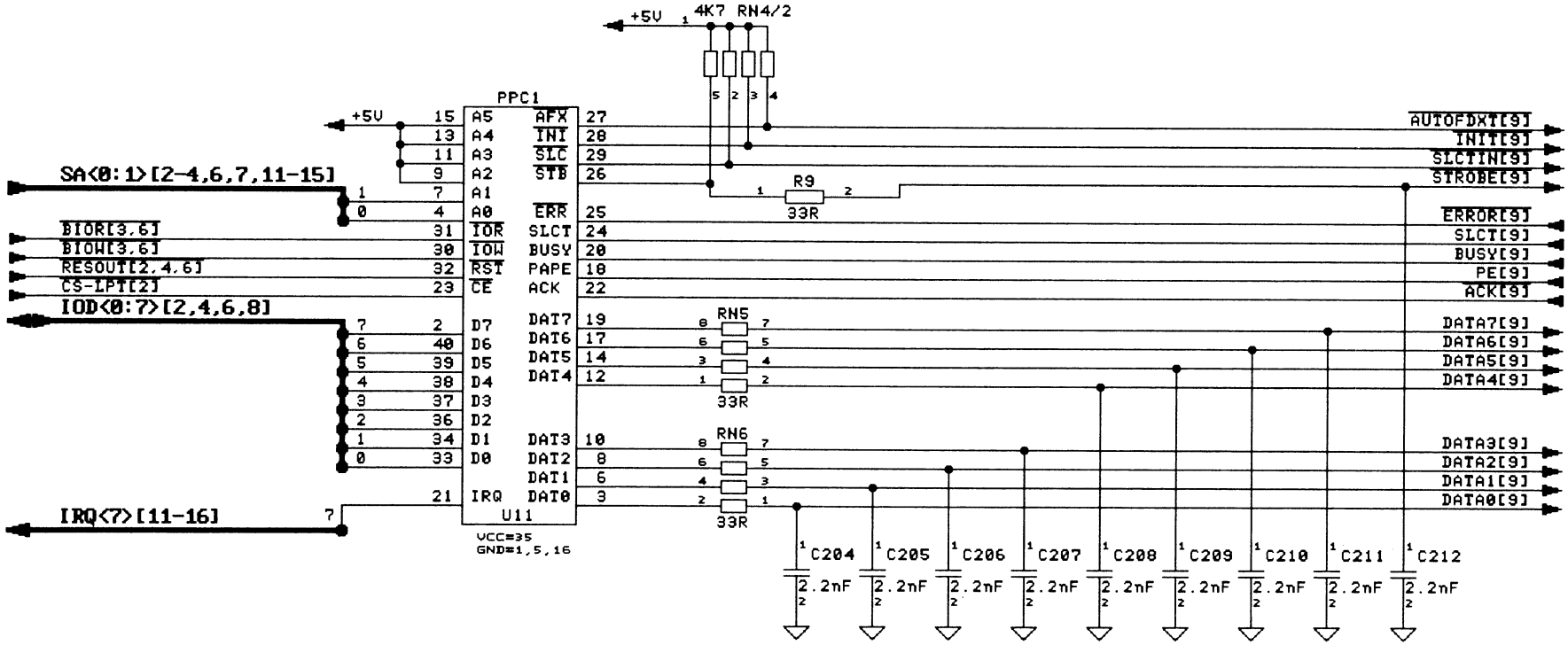
NOTES: 1) JS2 SELECTS WRITE PRECOMP. VAL.:
JS2 OPEN : 125 ns
JS2 CLOSED: 187 ns
2) JS3 SELECTS 2 SPEED SPINDLE DRIVE IF CLOSED
3) J15 SELECTS RPM POLARITY
JUMPER IN POS. 1-2: 1.2MB OR AT TYPE 1.44MB
JUMPER IN POS. 2-3: PS/2 TYPE 1.44MB
4) C104 IS BLOCK CAP TO OSC1
5) Q2, C102, C103 ONLY REQUIRED IF JS0A OPEN, JS0B CLOSED

TIO_83

Schneider			
DRAWN BY: B. ASSMANN	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 3 of 16		


SERIAL INTERFACE
+5V
4K7 RN4/1
COMOUT[2]
COMINT[2]
T1
BC337-16
R1
10K
D1
1N4148
R2
4K7
RI[9]
16450
RESETDRV[2,3,11-15]
RESOUT[2,5,6]
IOD<0:7>[2,5,6,8]
SA<0:2>[2,3,5-7,11-15]
CS-COM[2]
IOW-DLY[2]
IOR-DLY[2]
MR
CS0
CS1
D0
D1
D2
D3
D4
D5
D6
D7
DOSTR
DISTR
ADS
A0
A1
A2
CS2
XTAL1
XTAL2
RCLK
OUT2
INTRPT
OUT1
RI
DTR
RTS
SOUT
DDIS
CSOUT
NC
SIN
CTS
DSR
DCD
BAUDOUT
U8
VCC=40
GND=20
N/C
MC1488
U9/2
U9/3
U9/4
DTR[9]
RTS[9]
TXD[9]
MC1489
U10/1
U10/2
U10/3
U10/4
RXD[9]
CTS[9]
DSR[9]
DCD[9]
R7
1M
R8
1K
R10
1M
NOTE 2
Q1
1.8432 MHz
C100
22pF
C101
47pF
C105
330pF
C106
330pF
C107
330pF
C108
330pF
+12V
-12V
C120
100nF
C118
100nF
NOTE 1
NOTES: 1) C118 AND C120 ARE BLOCK CAPS FOR U9
2) R10 ASSEMBLED ONLY IF REQUIRED
TIO_84
Schneider
DRAWN BY: H. ULLRICH
APPROVED:
TITLE: SCHEMATIC TOWER-EGA/IO
USED ON: TOWER-AT
SIZE A3
50 228
REV 8
DATE: 11-18-88
SHEET: 4 of 16

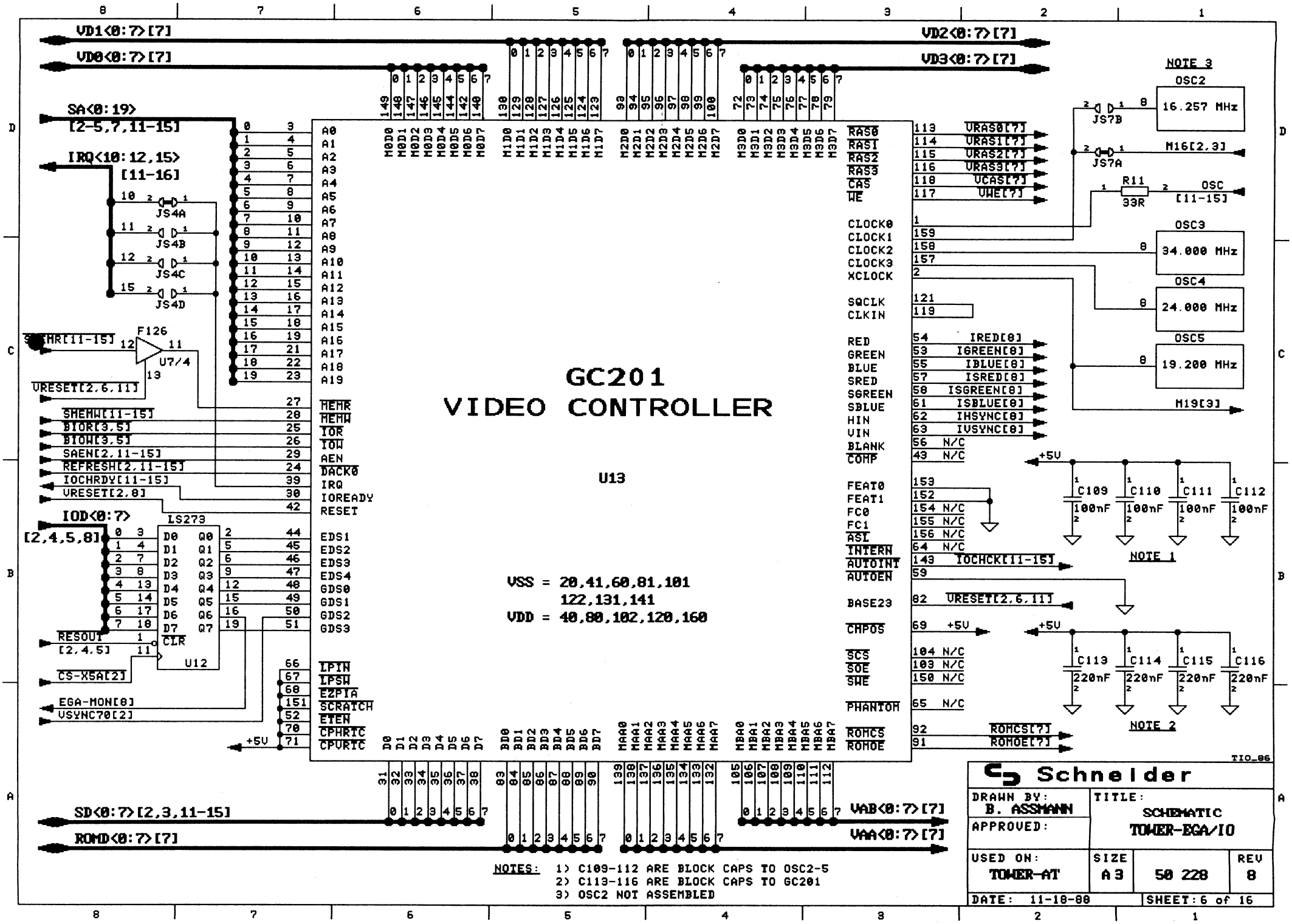
PARALLEL INTERFACE

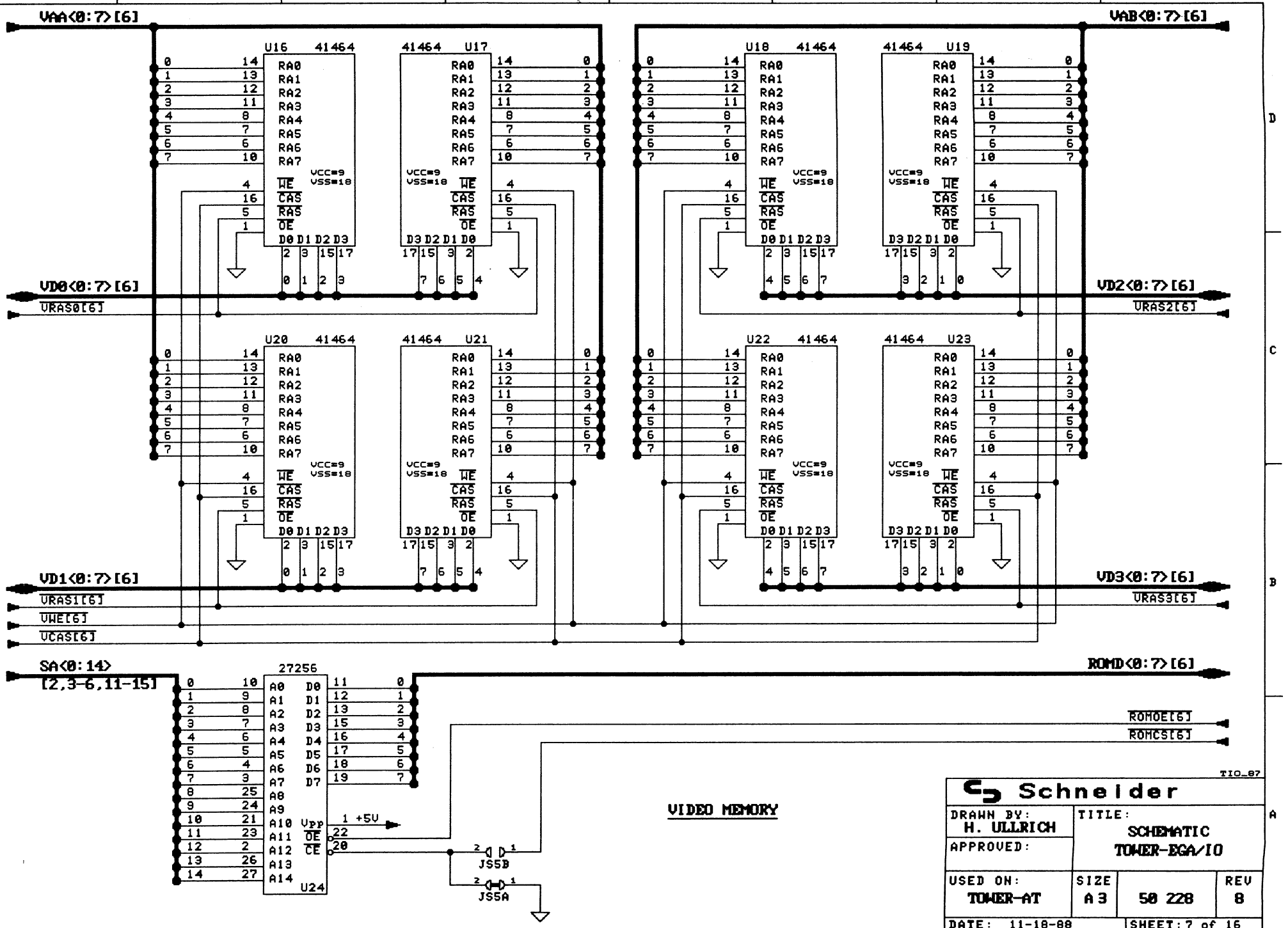


TIO_85

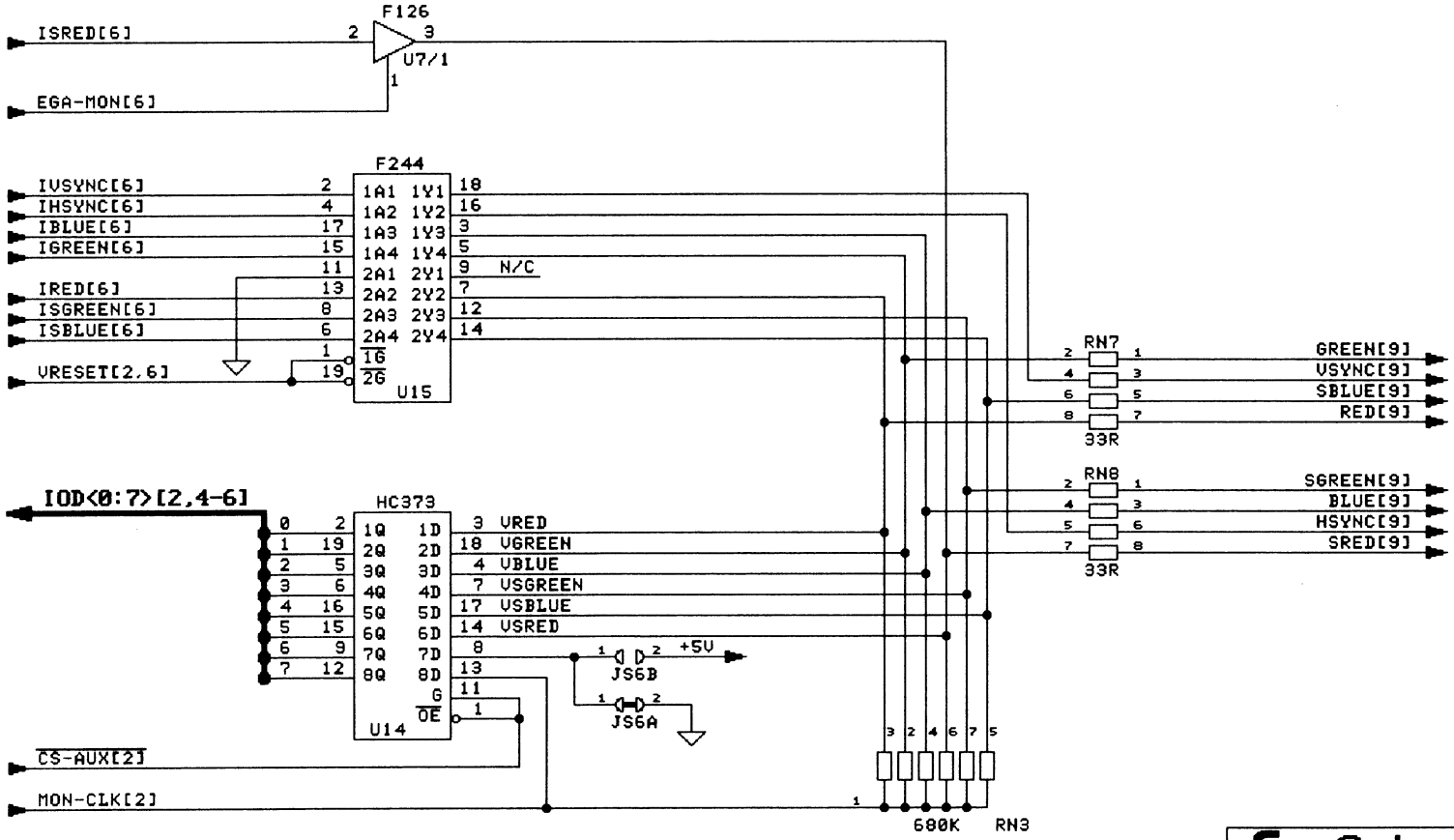
Schneider

DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 5 of 16		


GC201
VIDEO CONTROLLER
U13
VSS = 20,41,60,81,101
122,131,141
VDD = 40,80,102,120,160
VD1<0:7>[7]
VD0<0:7>[7]
VD2<0:7>[7]
VD3<0:7>[7]
SA<0:19>
[2-5,7,11-15]
IRQ<10:12,15>
[11-16]
JS4A
JS4B
JS4C
JS4D
F126
U7/4
VRESET[2,6,11]
SHEHR[11-15]
SHEHW[11-15]
BIOR[3,5]
BIOW[3,5]
SAEN[2,11-15]
REFRESH[2,11-15]
IOCHRDY[11-15]
VRESET[2,8]
IOD<0:7>
[2,4,5,8]
LS273
U12
RESOUT
[2,4,5]
CS-X5A[2]
EGA-MON[8]
VSYNC70[2]
+5V
MEMR
MEMW
IOR
IOW
AEN
DACK0
IRQ
IOREADY
RESET
EDS1
EDS2
EDS3
EDS4
GDS0
GDS1
GDS2
GDS3
IPIN
IPSW
EZPIA
SCRATCH
ETEN
CPHRTC
CPVRTC
SD<0:7>[2,3,11-15]
ROMD<0:7>[7]
VAB<0:7>[7]
VAA<0:7>[7]
URAS0[7]
URAS1[7]
URAS2[7]
URAS3[7]
UCAS[7]
UWE[7]
IRED[8]
IGREEN[8]
IBLUE[8]
ISRED[8]
ISGREEN[8]
ISBLUE[8]
IHSYNC[8]
IVSYNC[8]
IOCHCK[11-15]
VRESET[2,6,11]
ROMCS[7]
ROMOE[7]
NOTE 3
OSC2
16.257 MHz
JS7B
JS7A
M16[2,3]
R11
33R
OSC
[11-15]
OSC3
34.000 MHz
OSC4
24.000 MHz
OSC5
19.200 MHz
M19[3]
C109
C110
C111
C112
100nF
NOTE 1
C113
C114
C115
C116
220nF
NOTE 2
TIO_86
NOTES: 1) C109-112 ARE BLOCK CAPS TO OSC2-5
2) C113-116 ARE BLOCK CAPS TO GC201
3) OSC2 NOT ASSEMBLED
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC TOWER-EGA/IO
USED ON: TOWER-AT
SIZE A3
50 228
REV 8
DATE: 11-18-88
SHEET: 6 of 16


VAA<0:7>[6]
VAB<0:7>[6]
U16 41464
41464 U17
U18 41464
41464 U19
U20 41464
41464 U21
U22 41464
41464 U23
RA0
RA1
RA2
RA3
RA4
RA5
RA6
RA7
VCC=9
VSS=18
WE
CAS
RAS
OE
D0 D1 D2 D3
VD0<0:7>[6]
VD2<0:7>[6]
VD1<0:7>[6]
VD3<0:7>[6]
URAS0[6]
URAS2[6]
URAS1[6]
URAS3[6]
UWE[6]
UCAS[6]
SA<0:14>
[2,3-6,11-15]
27256
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
D0
D1
D2
D3
D4
D5
D6
D7
Vpp
OE
CE
U24
+5V
JS5B
JS5A
ROMD<0:7>[6]
ROMOE[6]
ROMCS[6]
VIDEO MEMORY
TIO_87
Schneider
DRAWN BY: H. ULLRICH
APPROVED:
TITLE: SCHEMATIC TOWER-EGA/IO
USED ON: TOWER-AT
SIZE A3
50 228
REV 8
DATE: 11-18-88
SHEET: 7 of 16

VIDEO INTERFACE



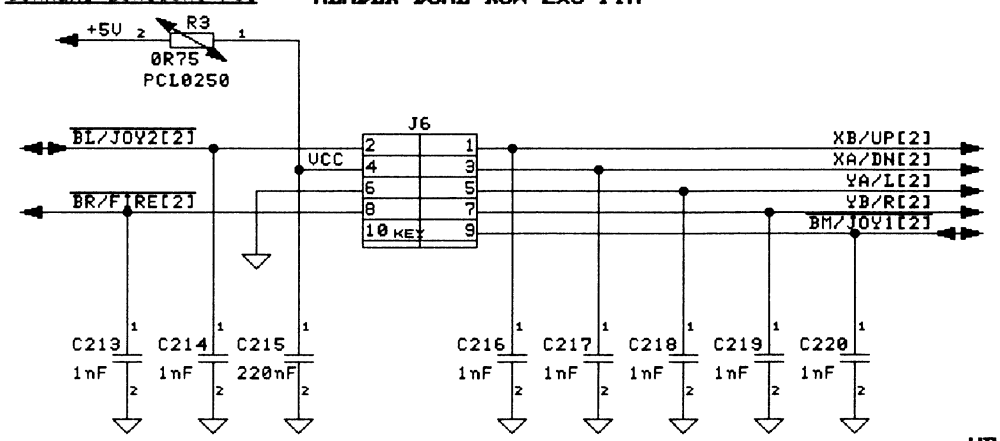
TIO_88

Schneider			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 8 of 16		

MOUSE/JOYSTICK

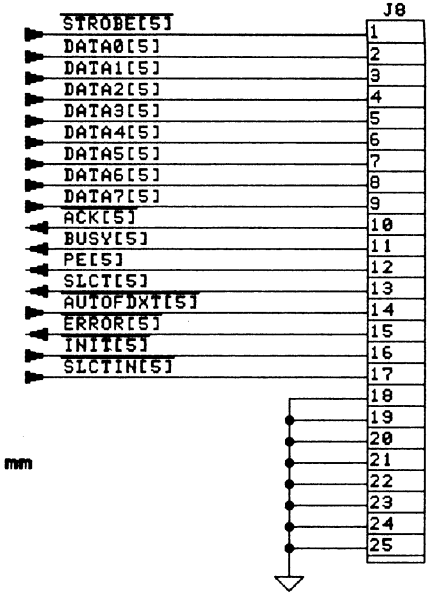
HEADER DUAL ROW 2x5 PIN

CURRENT LIMITING PTC



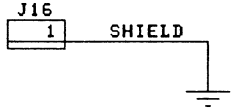
PARALLEL PORT

25 PIN SUBD CONN. FEMALE



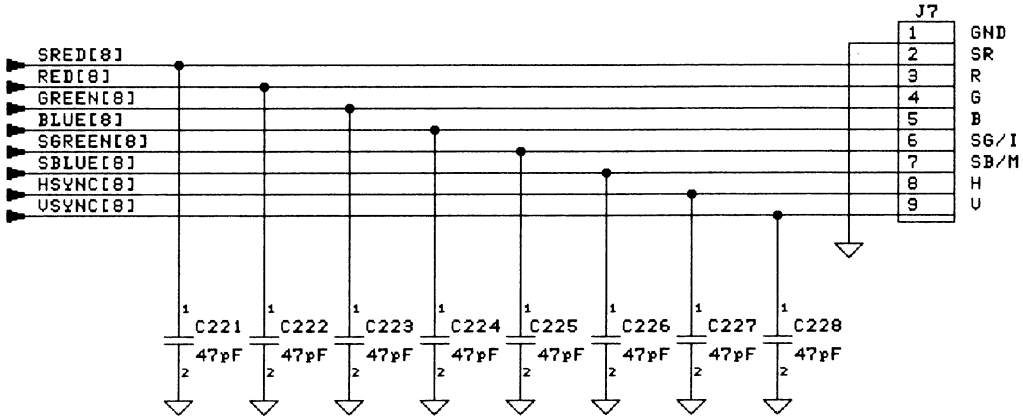
SHIELD CONNECTOR

HEADE5 FASTON 2,8 x 0.8 mm



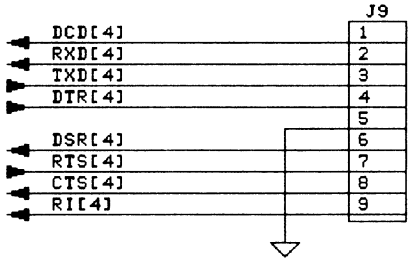
VIDEO MONO/RGB

9 PIN SUBD CONN. FEMALE



SERIAL PORT

9 PIN SUBD CONN. MALE



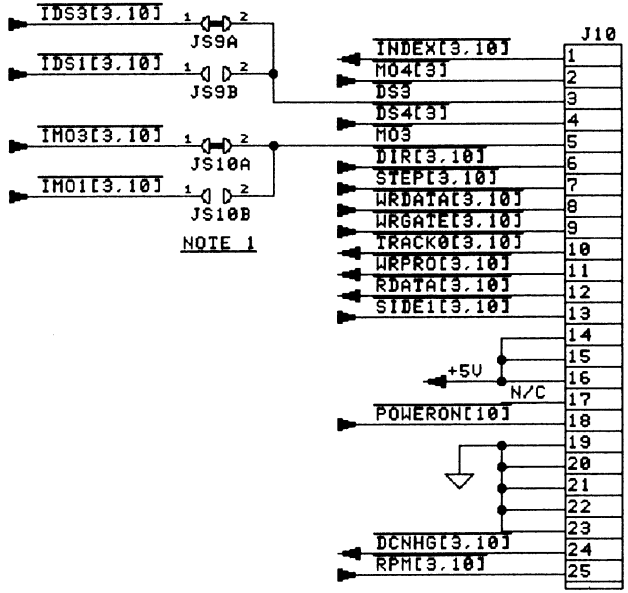
CONNECTORS I

TIO_89

Schneider			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 9 of 16		

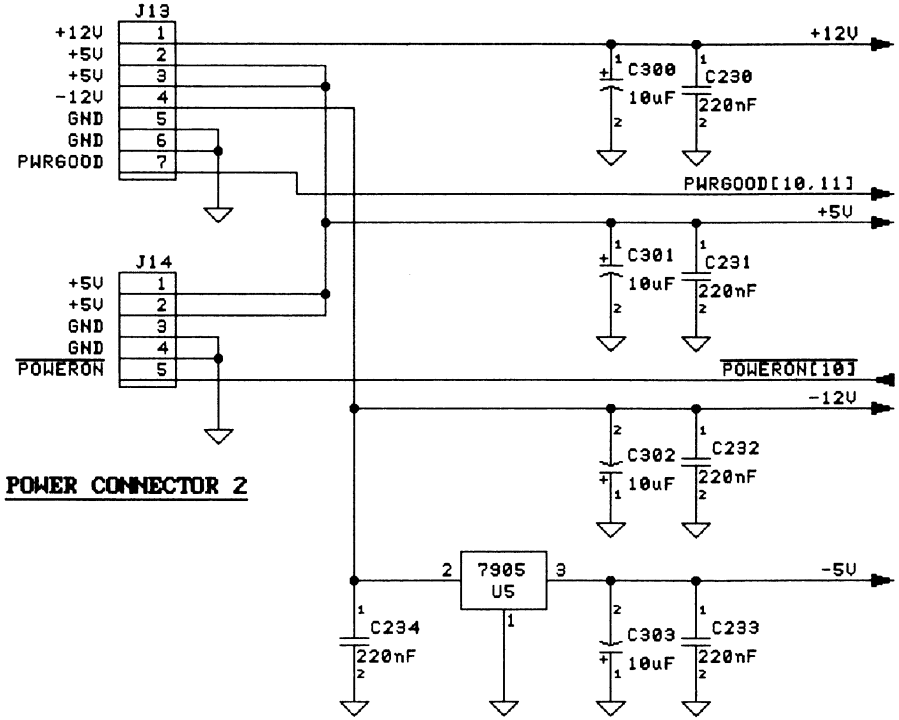
FLOPPY EXTERN

25 PIN SUBD CONN. FEMALE



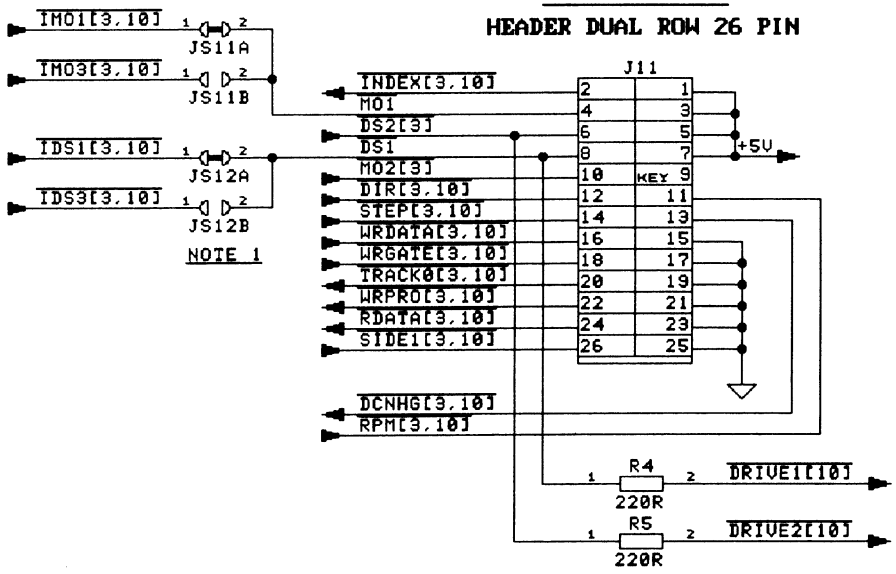
POWER CONNECTOR 1

POWER CONNECTOR 2



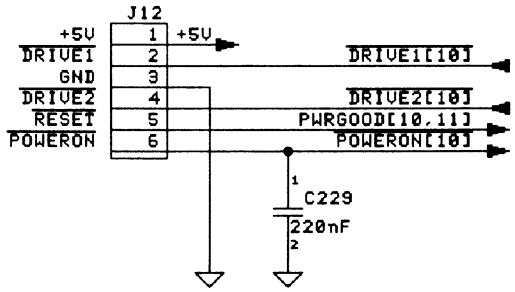
FLOPPY INTERN

HEADER DUAL ROW 26 PIN



LED CONNECTOR

HEADER MICRO MATCH 6 PIN



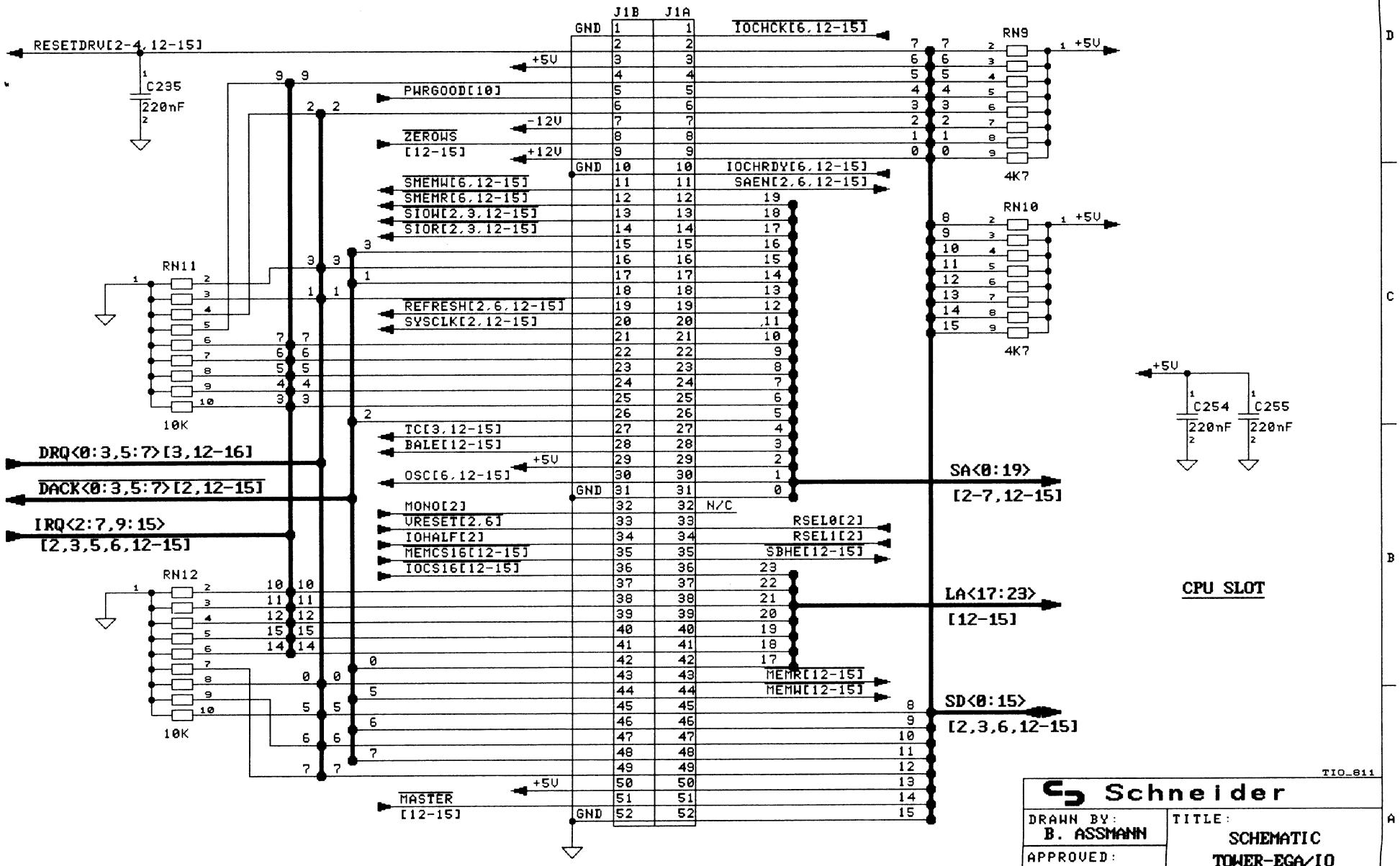
CONNECTORS II

NOTES: 1) JS9-12 ALLOW TO PHYSICALLY ALTER DRIVE 1 (NORMALLY INTERN) AND DRIVE 3 (NORMALLY EXTERN) E.G. TO ALLOW BOOTING FROM EXTERNAL 5.25" 1.2MB DRIVE. IN THIS CASE JS9-12 A JUMPERS MUST BE CUT AND JS9-12 B JUMPERS MUST BE CLOSED.

TIO_810

Schneider

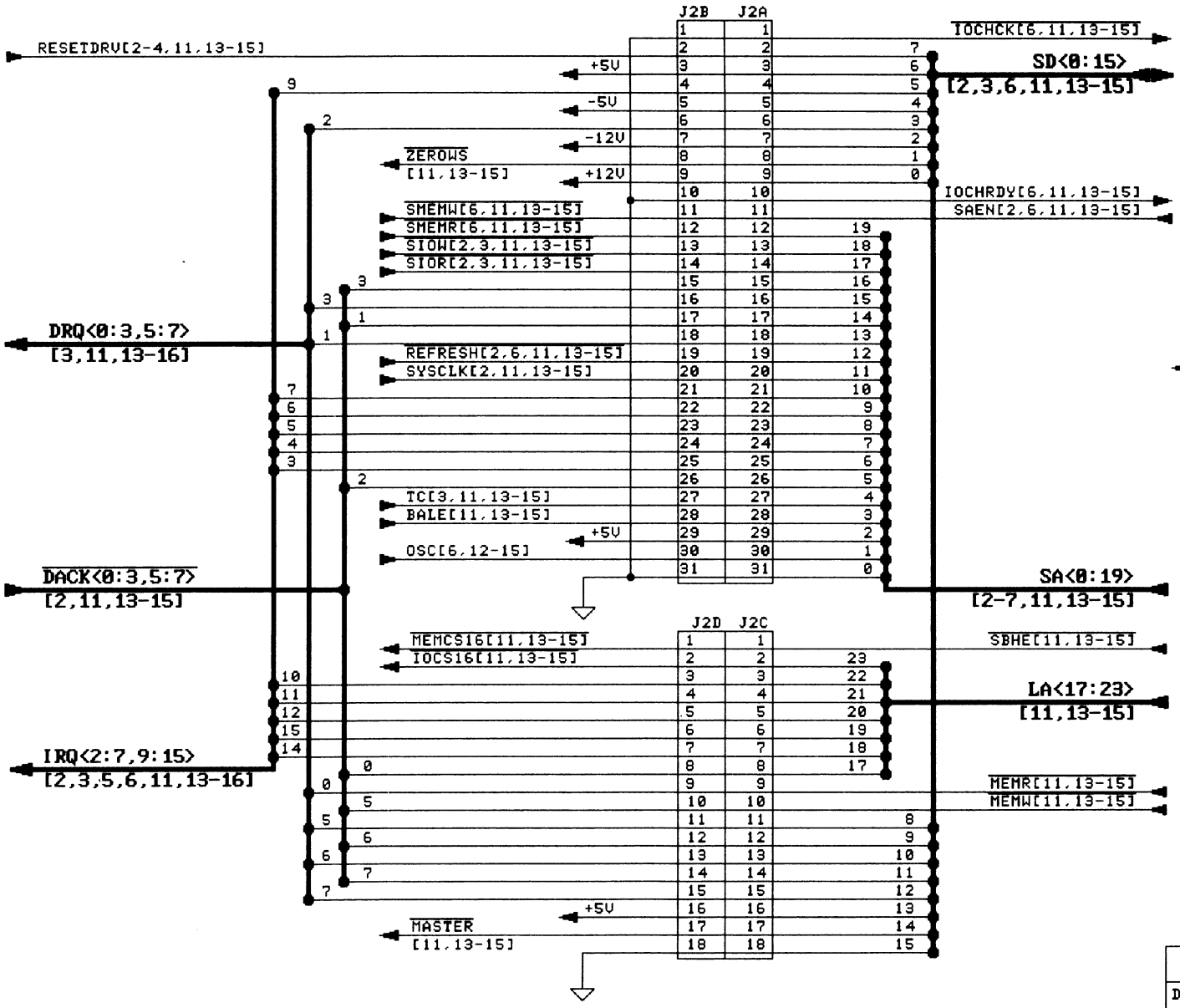
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 10 of 16		

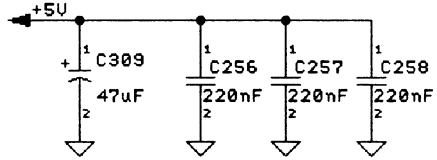


TIO_811

Schneider

DRAWN BY: B. ASSMANN	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50'228	REV 8
DATE: 11-18-88	SHEET: 11 of 16		

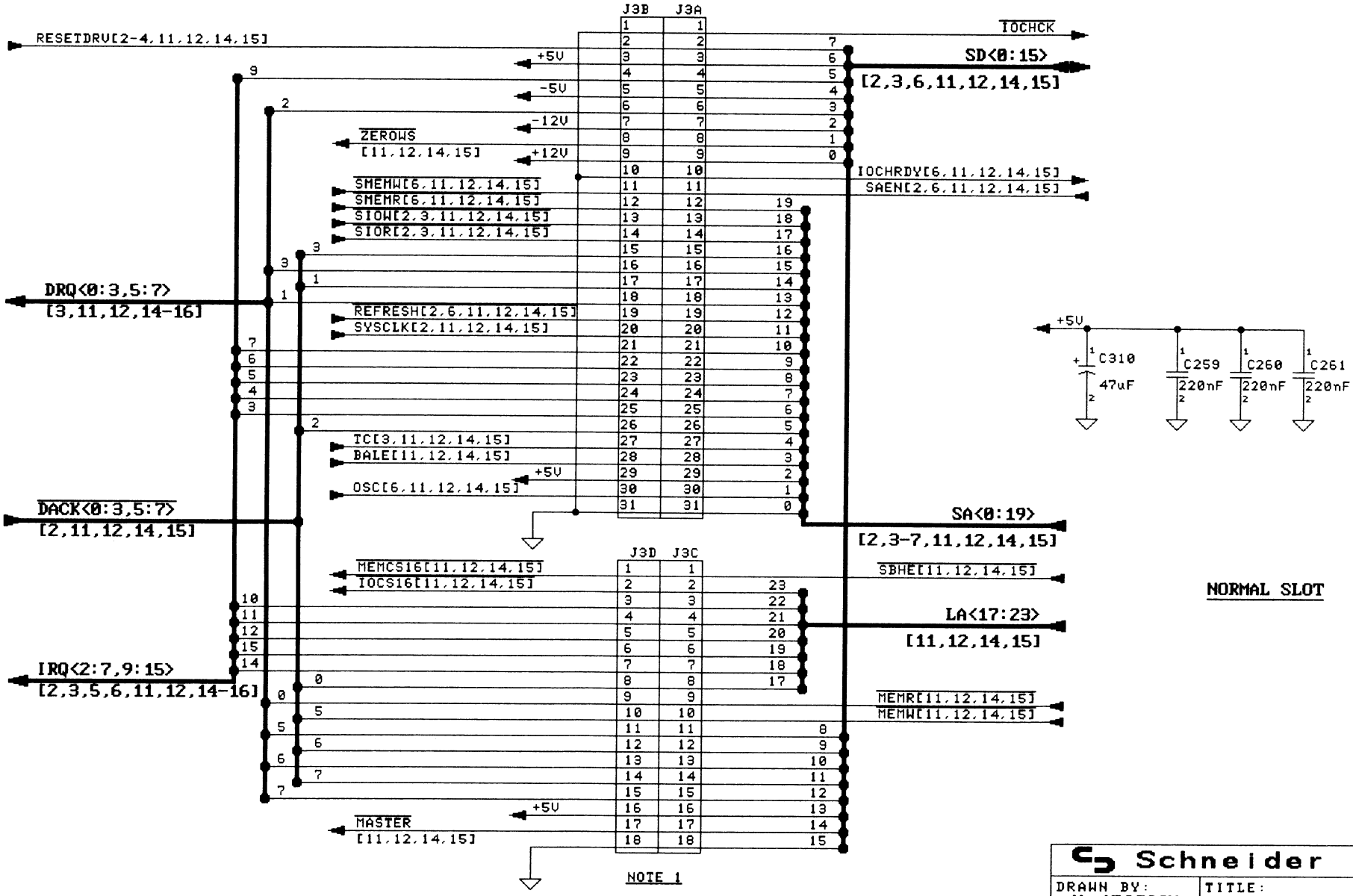




NORMAL SLOT

TIO_812

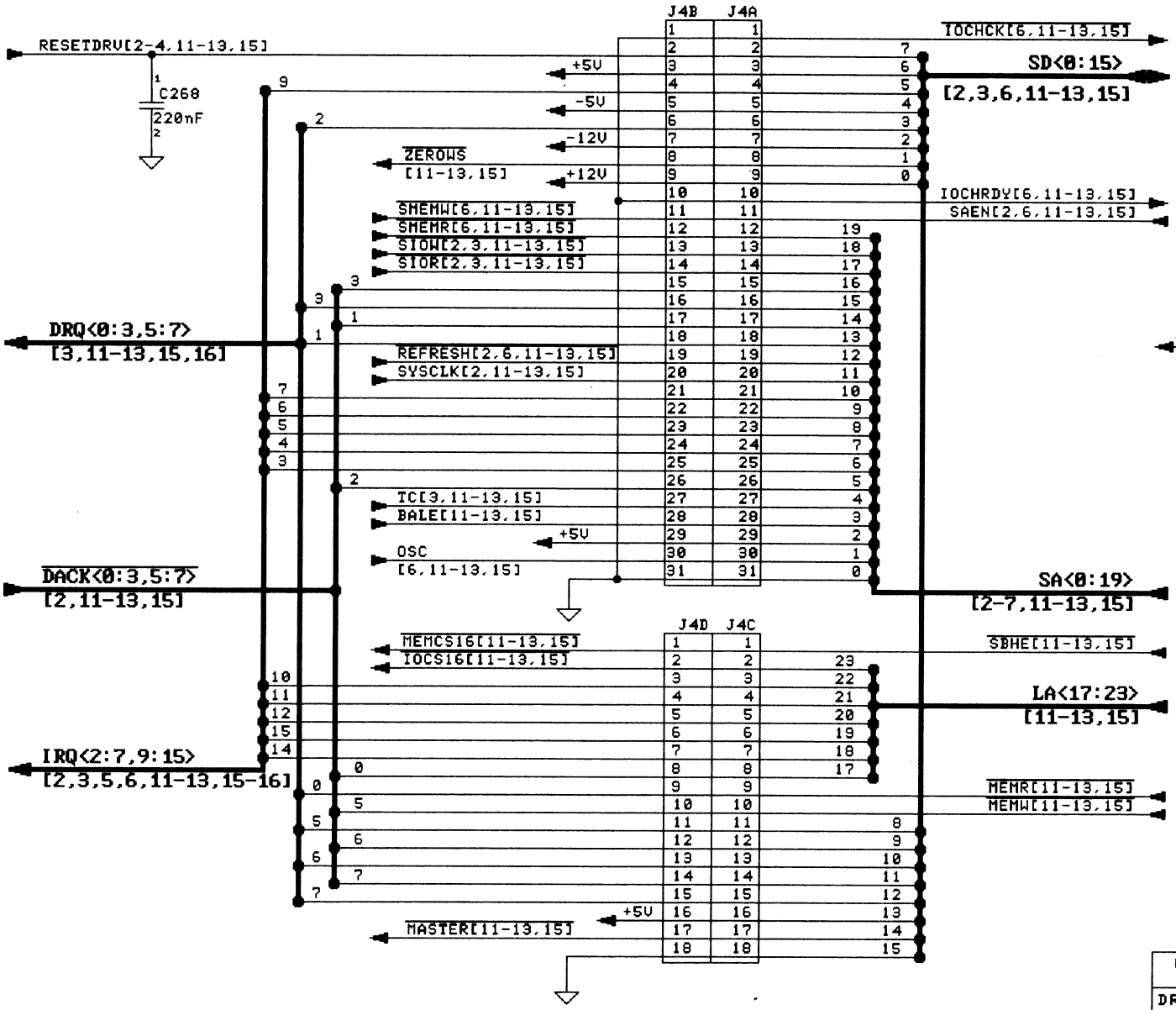
Schneider			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 12 of 16		



NOTES: 1) CARDEDGE CONNECTOR J3C-D NOT ASSEMBLED

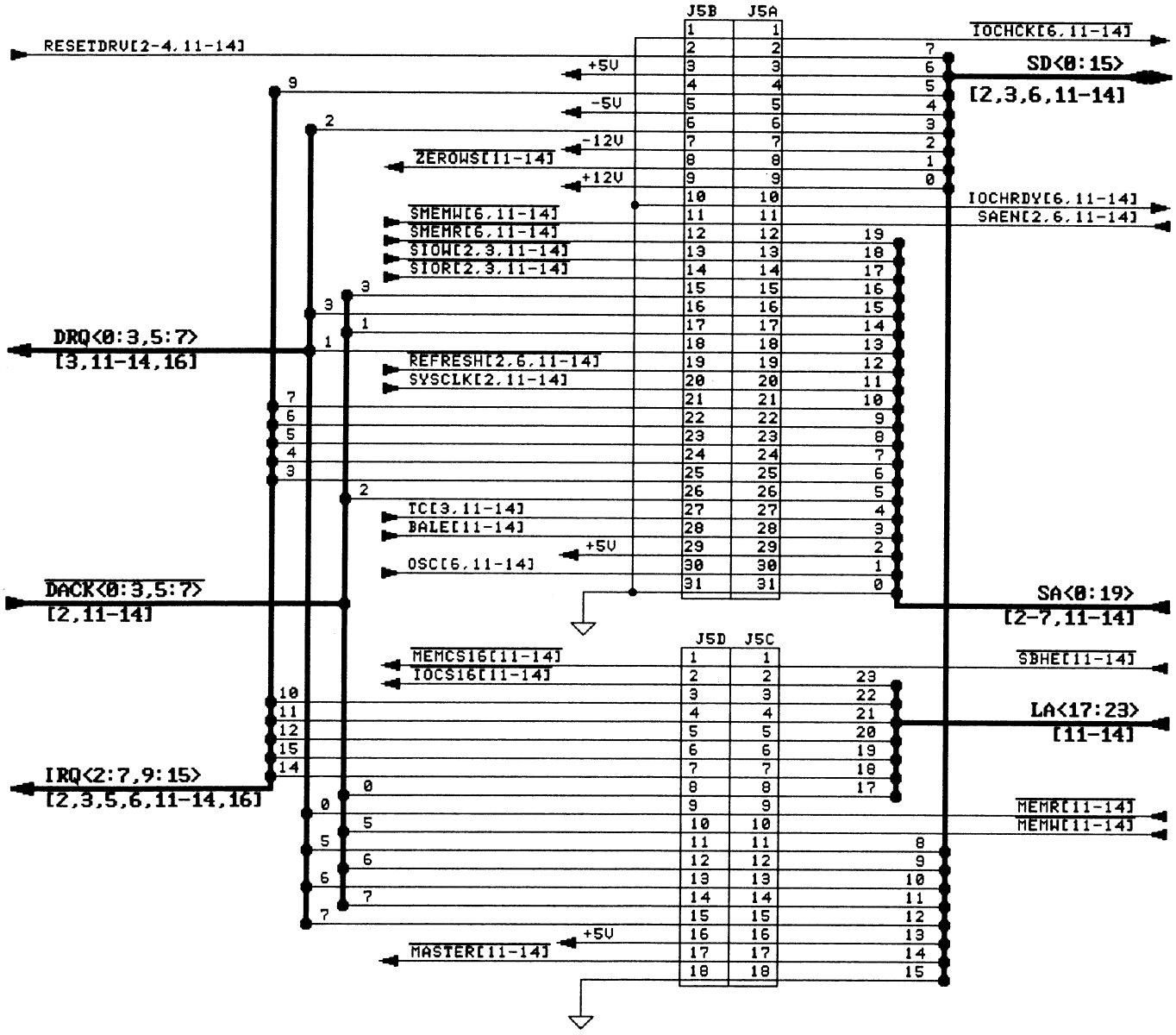
TIO_813

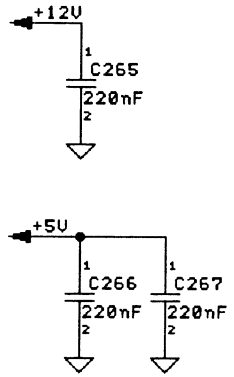
Schneider			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 13 of 16		



TIO_814

Schneider			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 14 of 16		





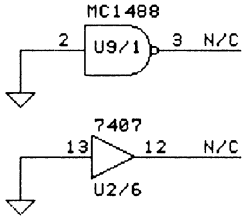
NORMAL SLOT

TIO_815

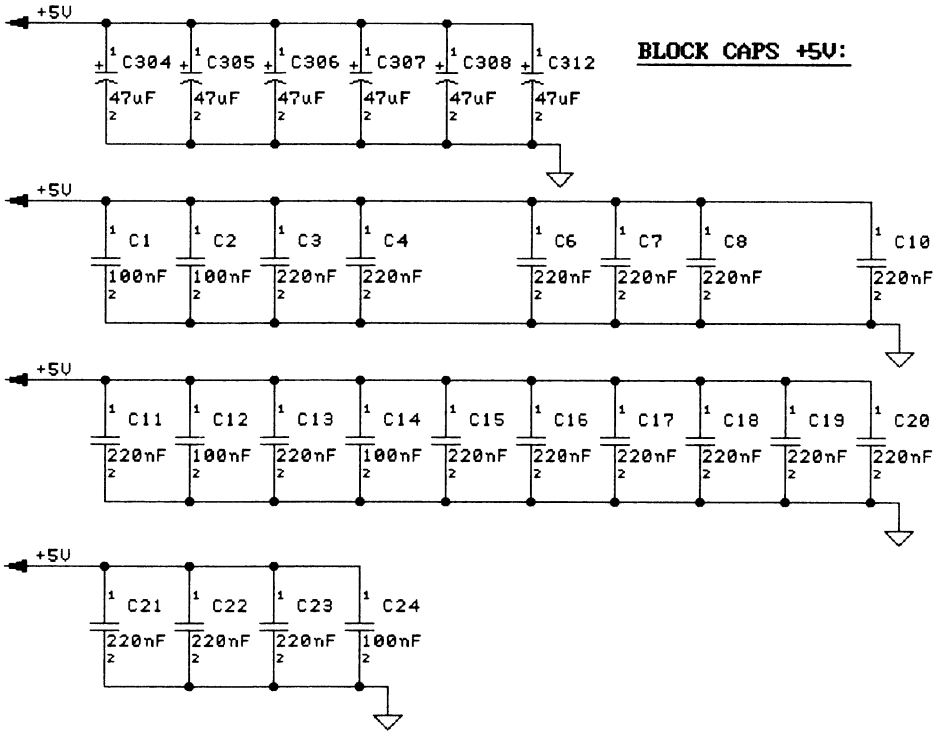
Schneider

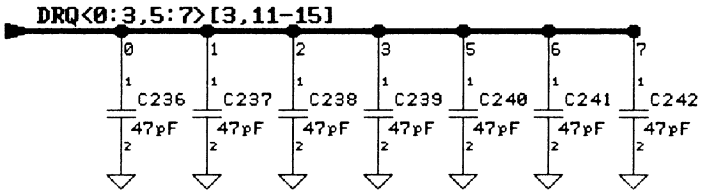
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 15 of 16		

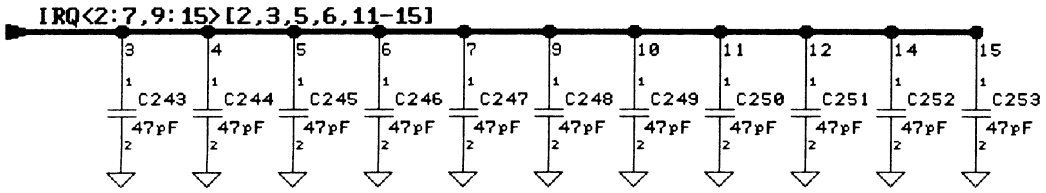
SPARE GATES



BLOCK CAPS +5V:







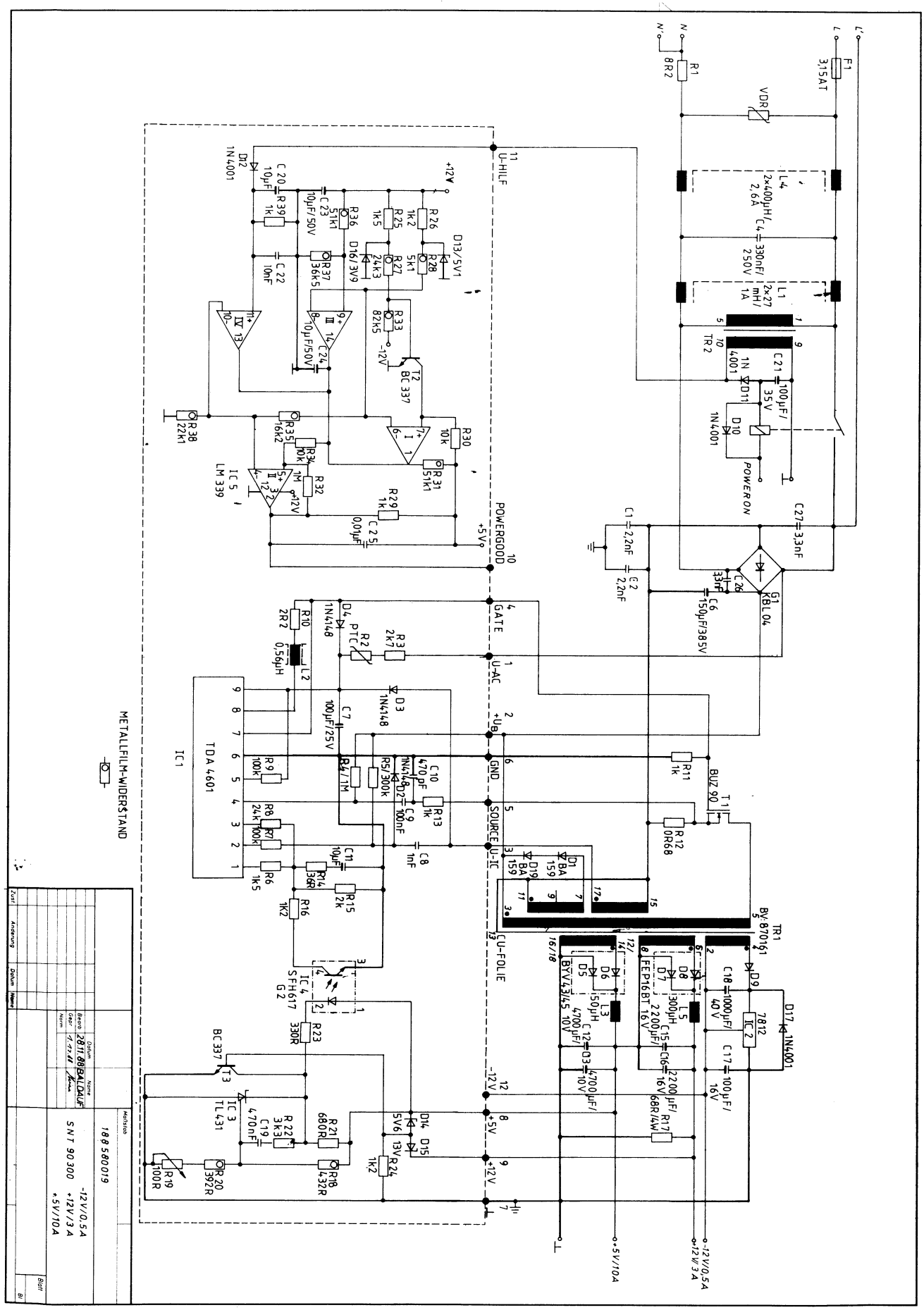
TIO_816

Schneider

DRAWN BY: B. ASSMANN	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 228	REV 8
DATE: 11-18-88	SHEET: 16 of 16		

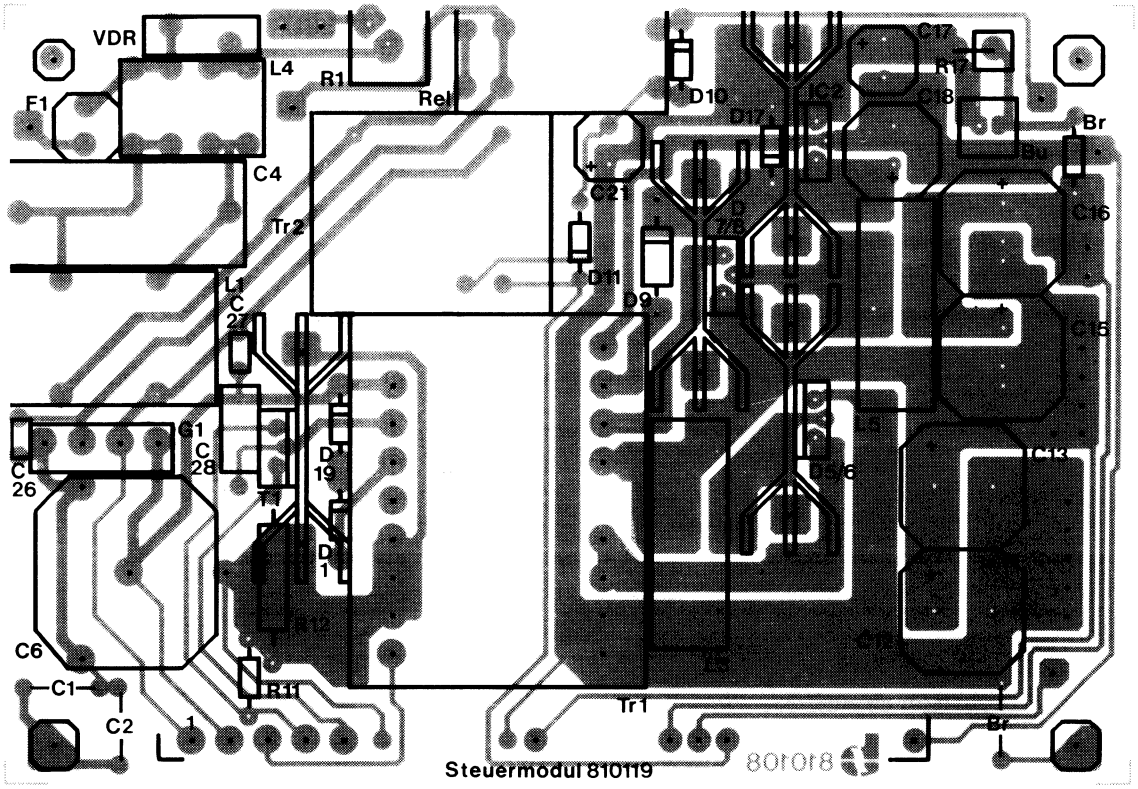
Schematic diagram

Power supply SCD–SNT 90/B03

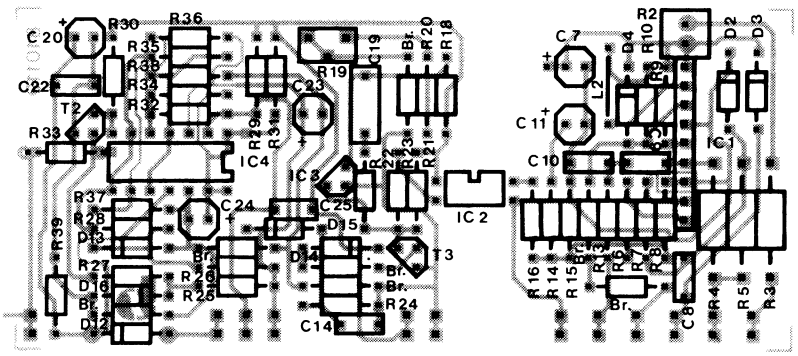


Power supply SCD–SNT 90/B03

Component side

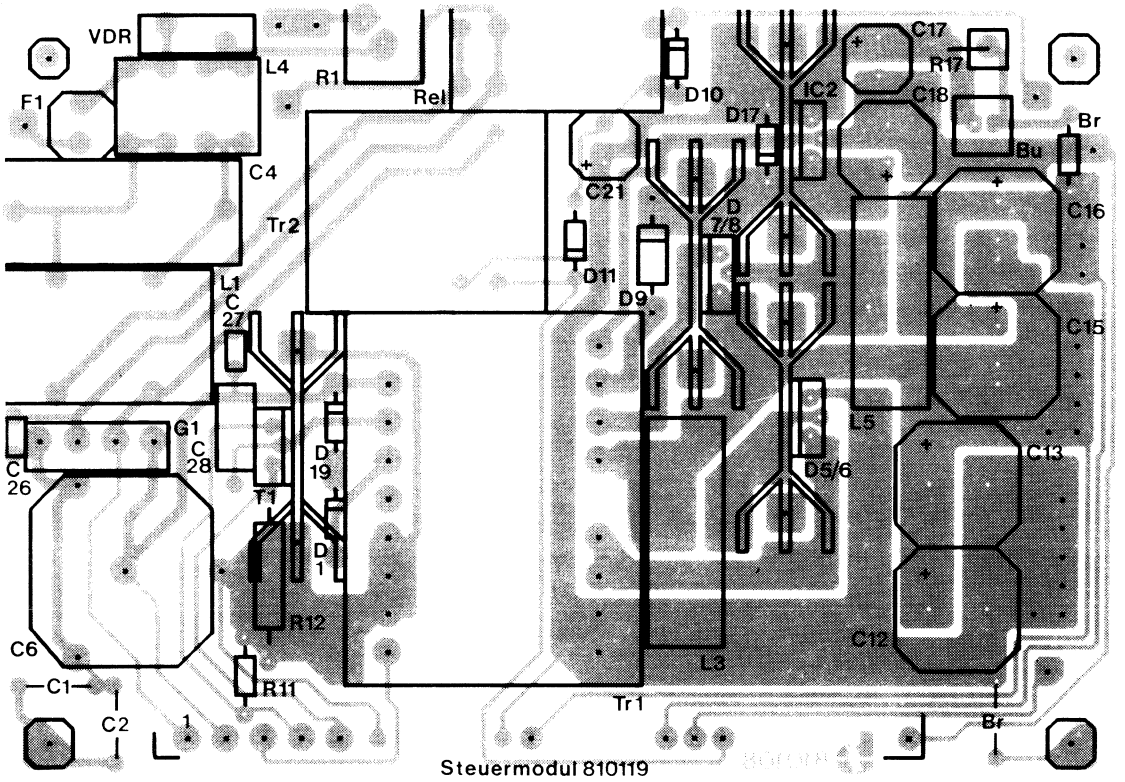


Schaltnetzteil „Tower" SCD-SNT 90/01 B03 Id.580018 Ident Nr.7270-50215



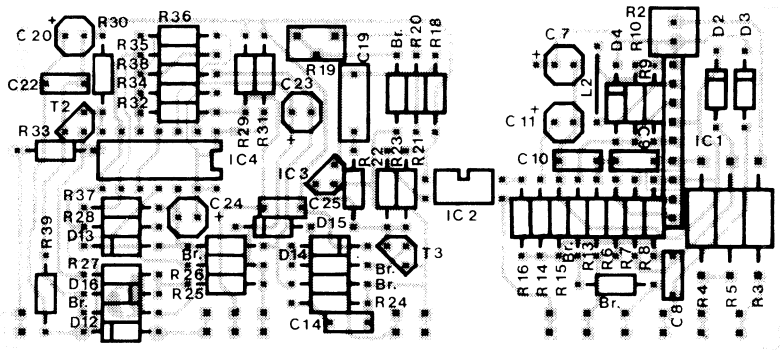
Power supply SCD-SNT 90/B03

Component side



Steuermodul 810119

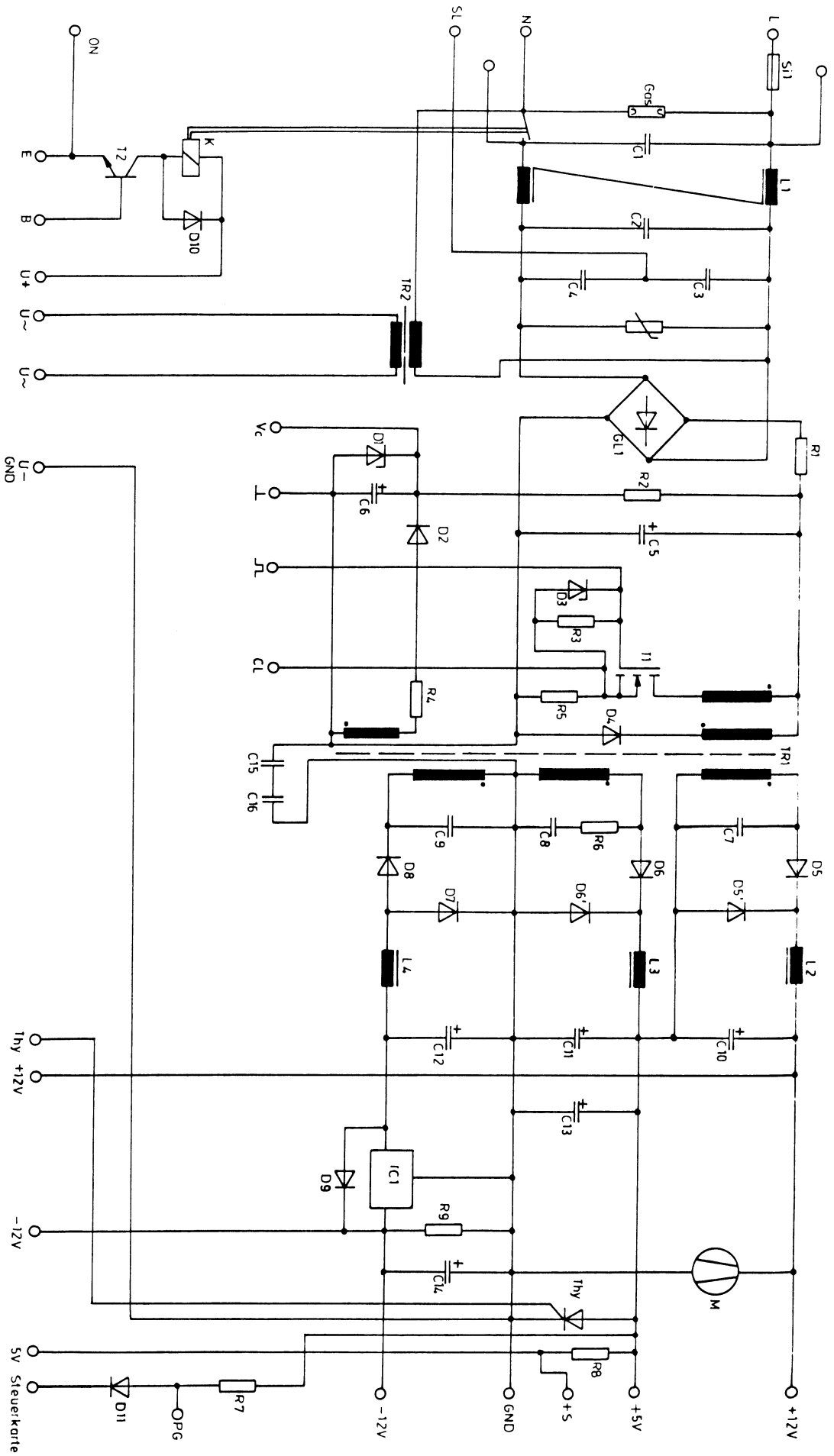
Schaltnetzteil „Tower" SCD-SNT 90/01 B03 Id.580018 Ident Nr.7270-50215



Steuermodul 810119

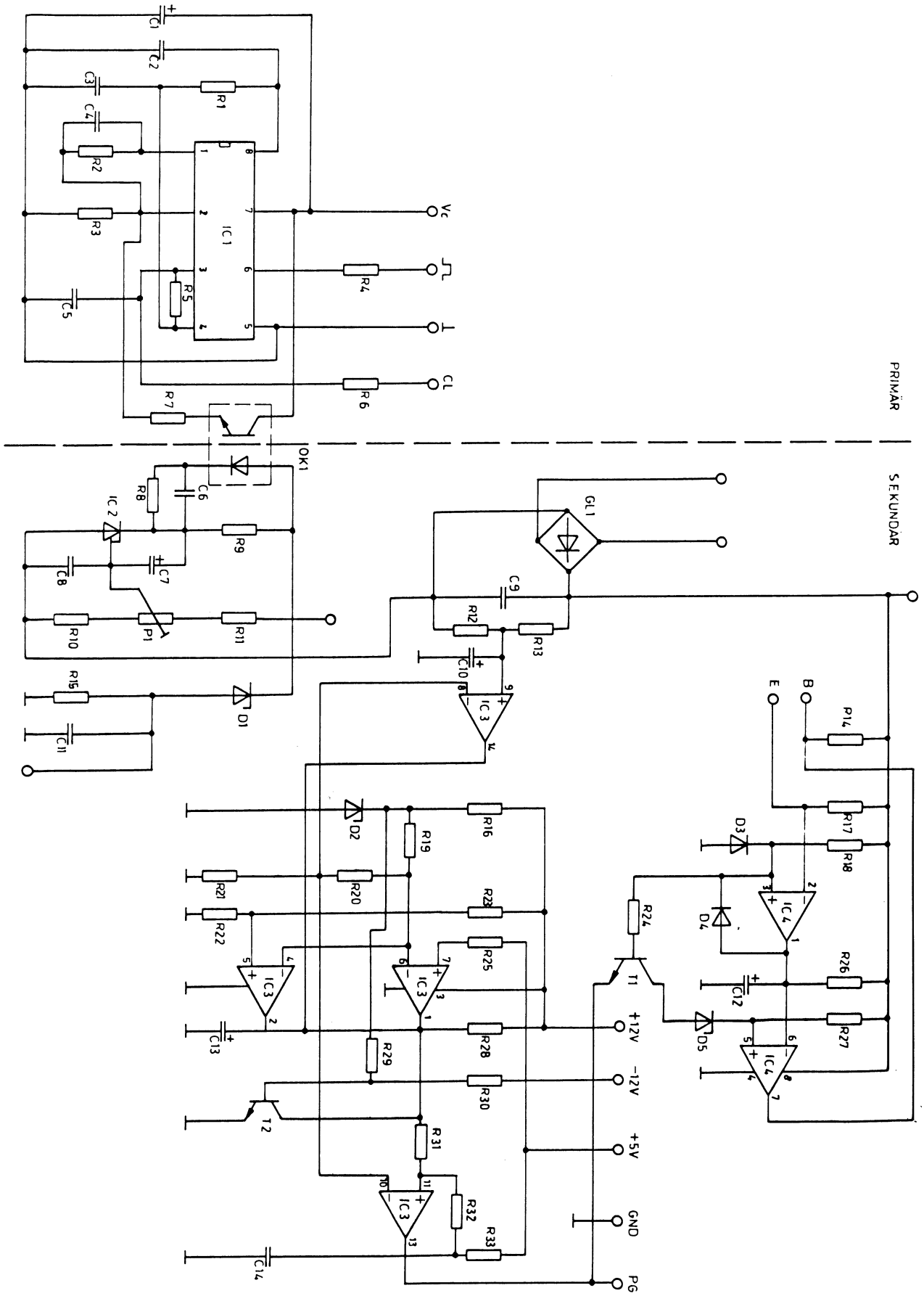
Schematic diagram

Power supply SCD–SNT 90/B03
Mainboard



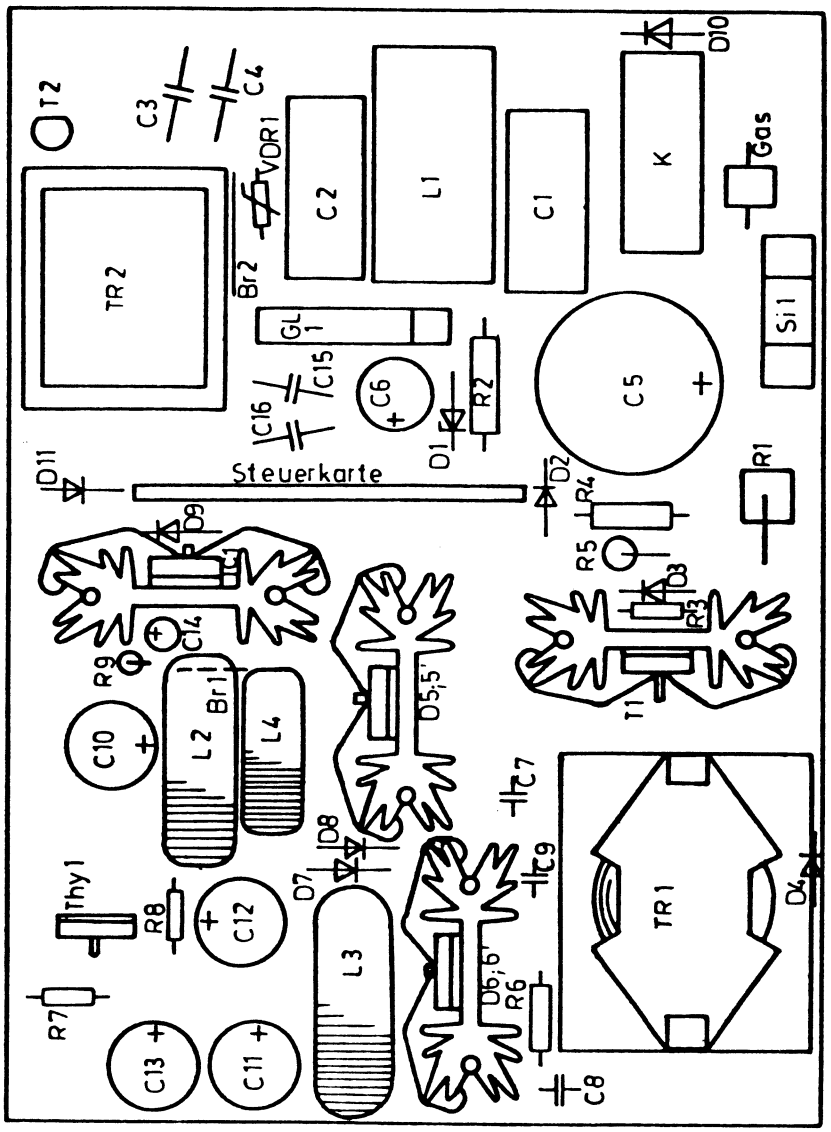
Schematic diagram

Power supply SCD–SNT 90/E02
Controlboard

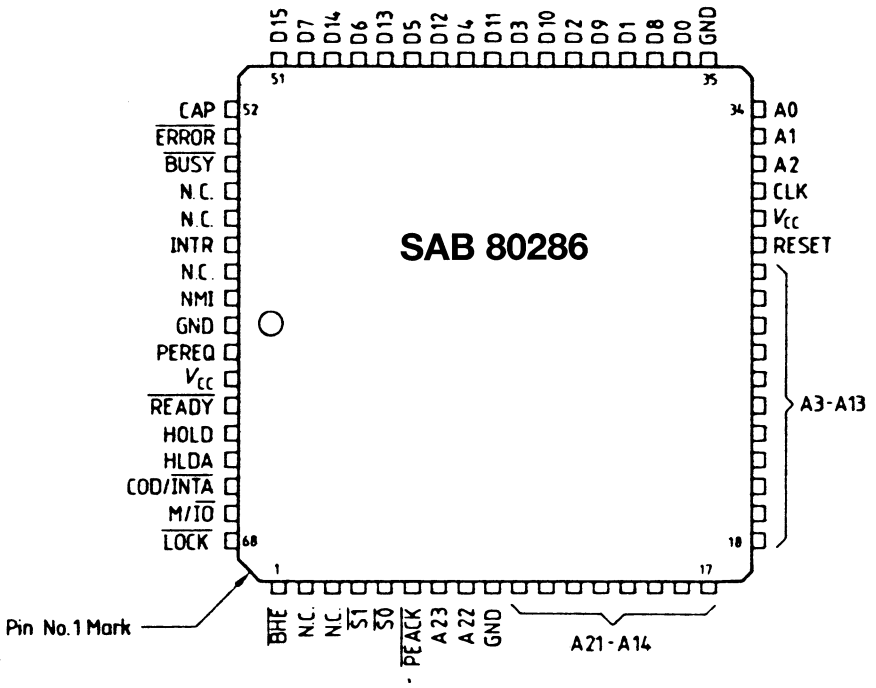


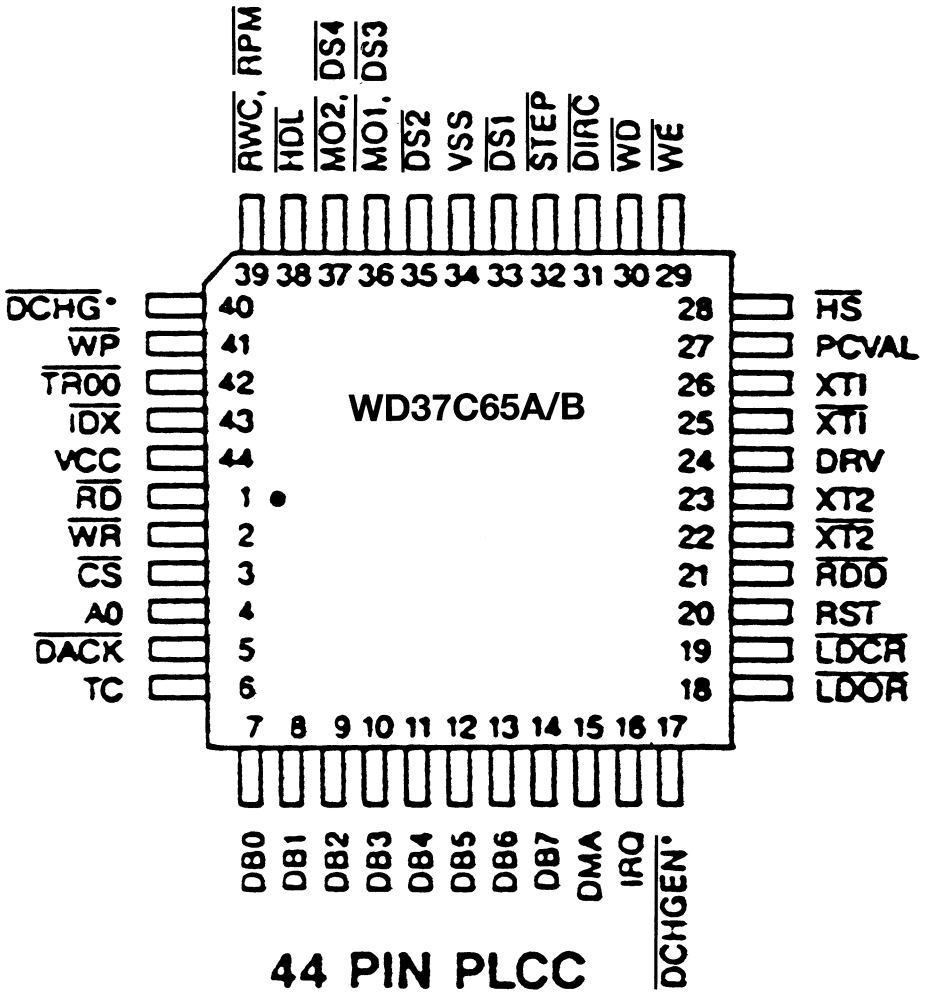
Power supply SCD–SNT 90/E02

Component side

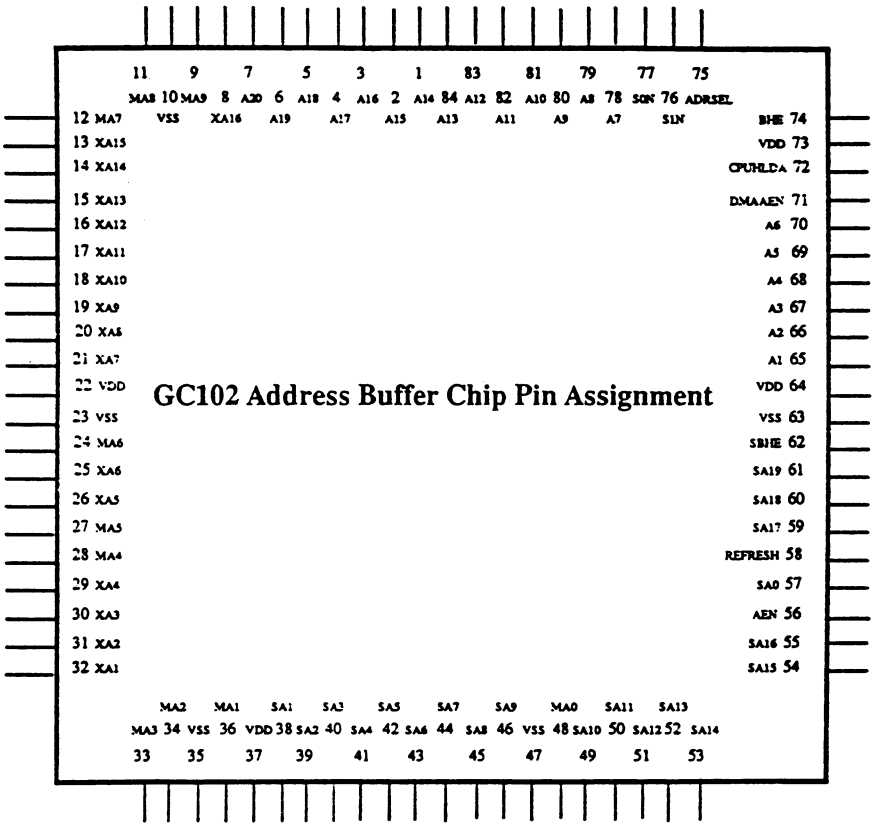


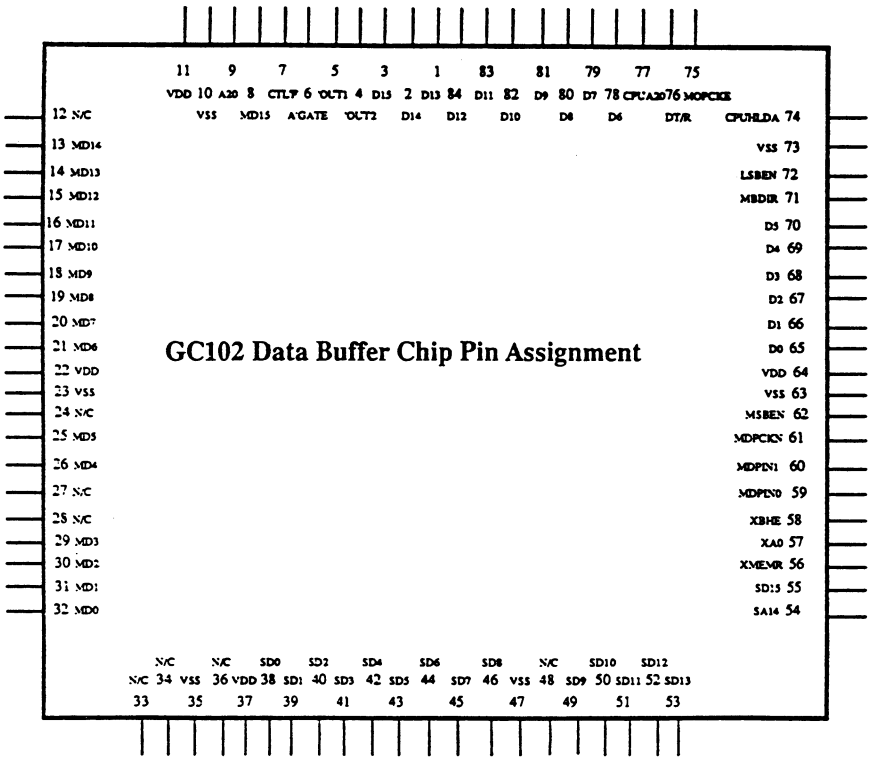
Pin assignment





Pin assignment





Pin assignment

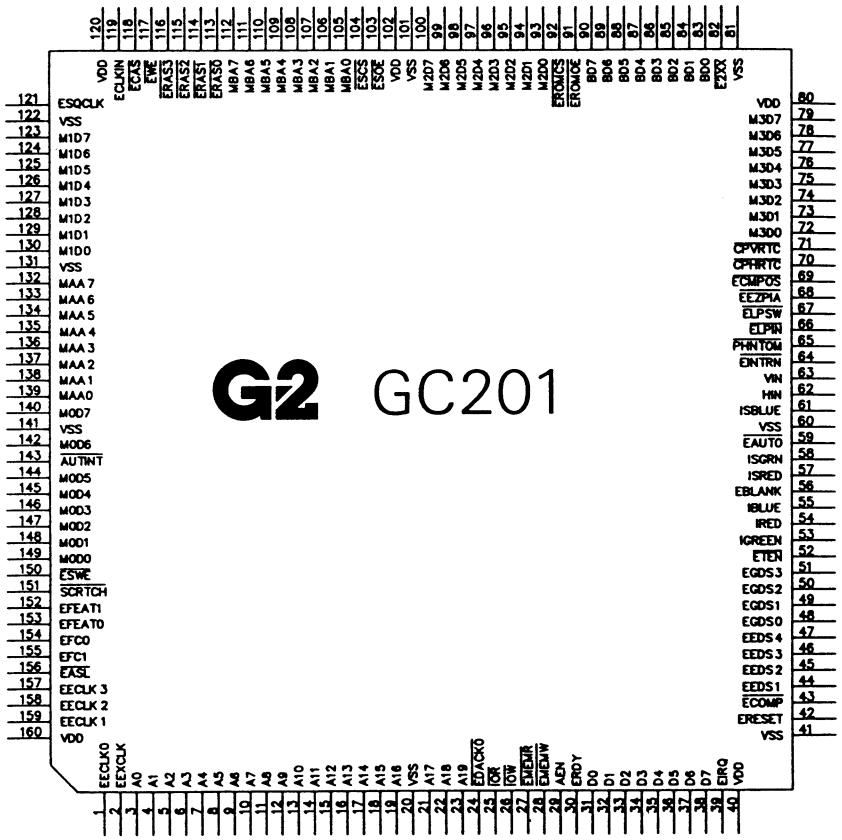
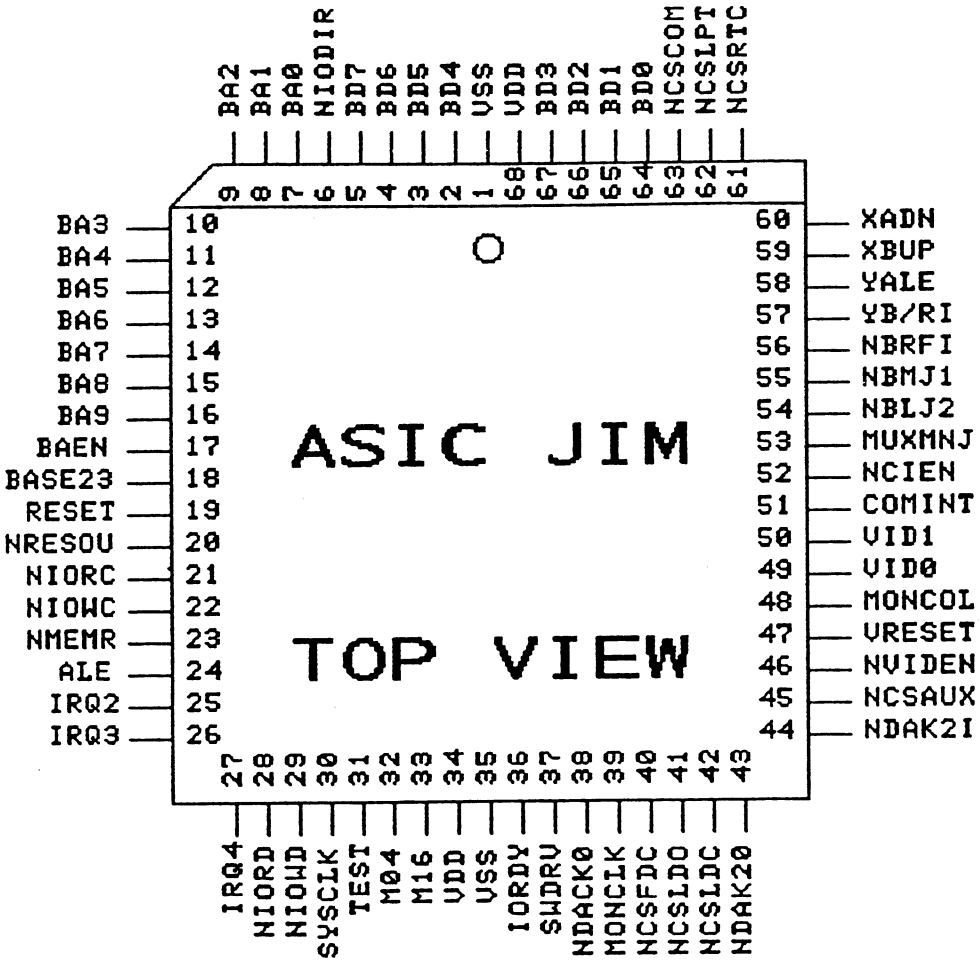
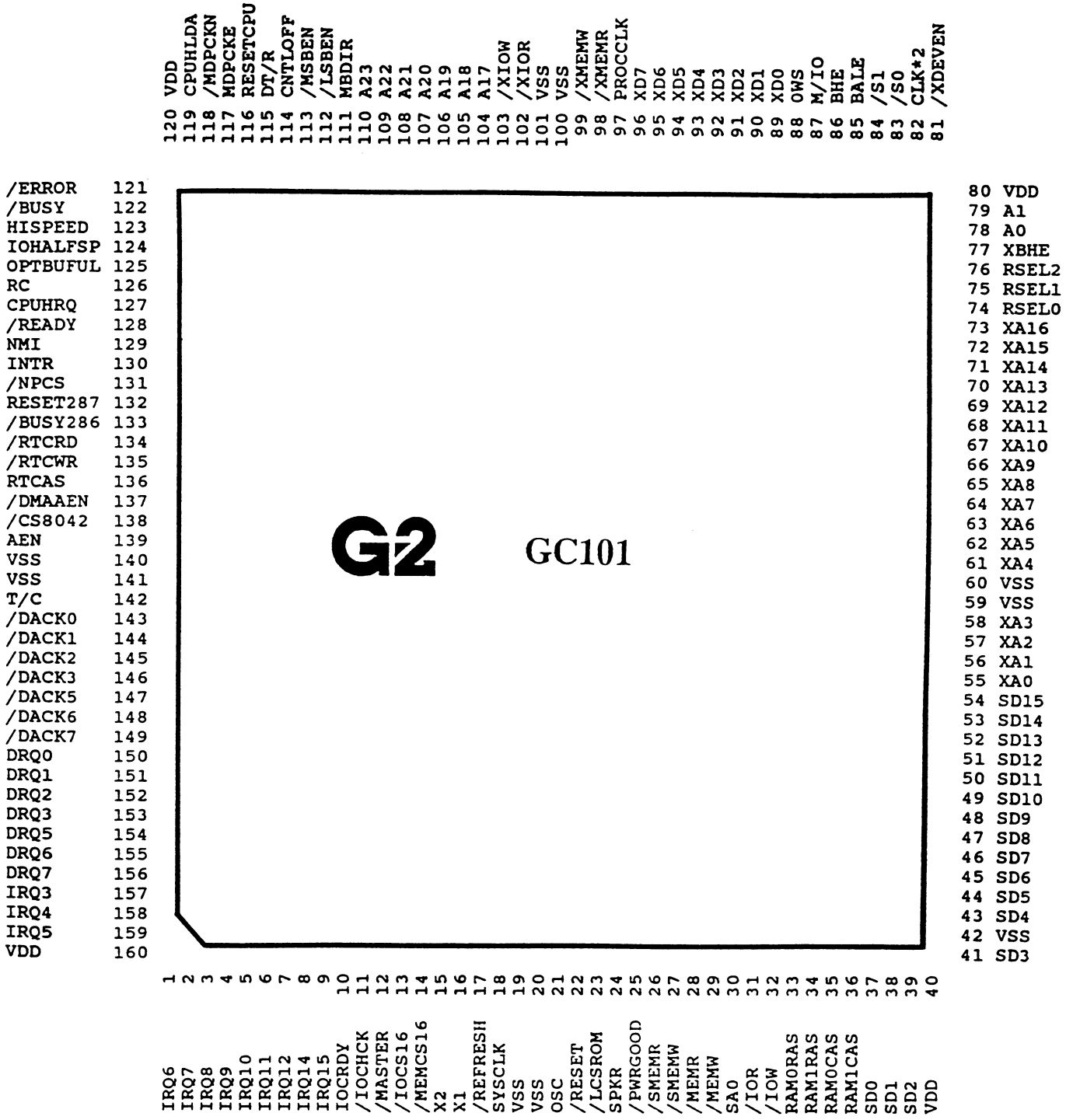


Figure 2 Pin Assignment

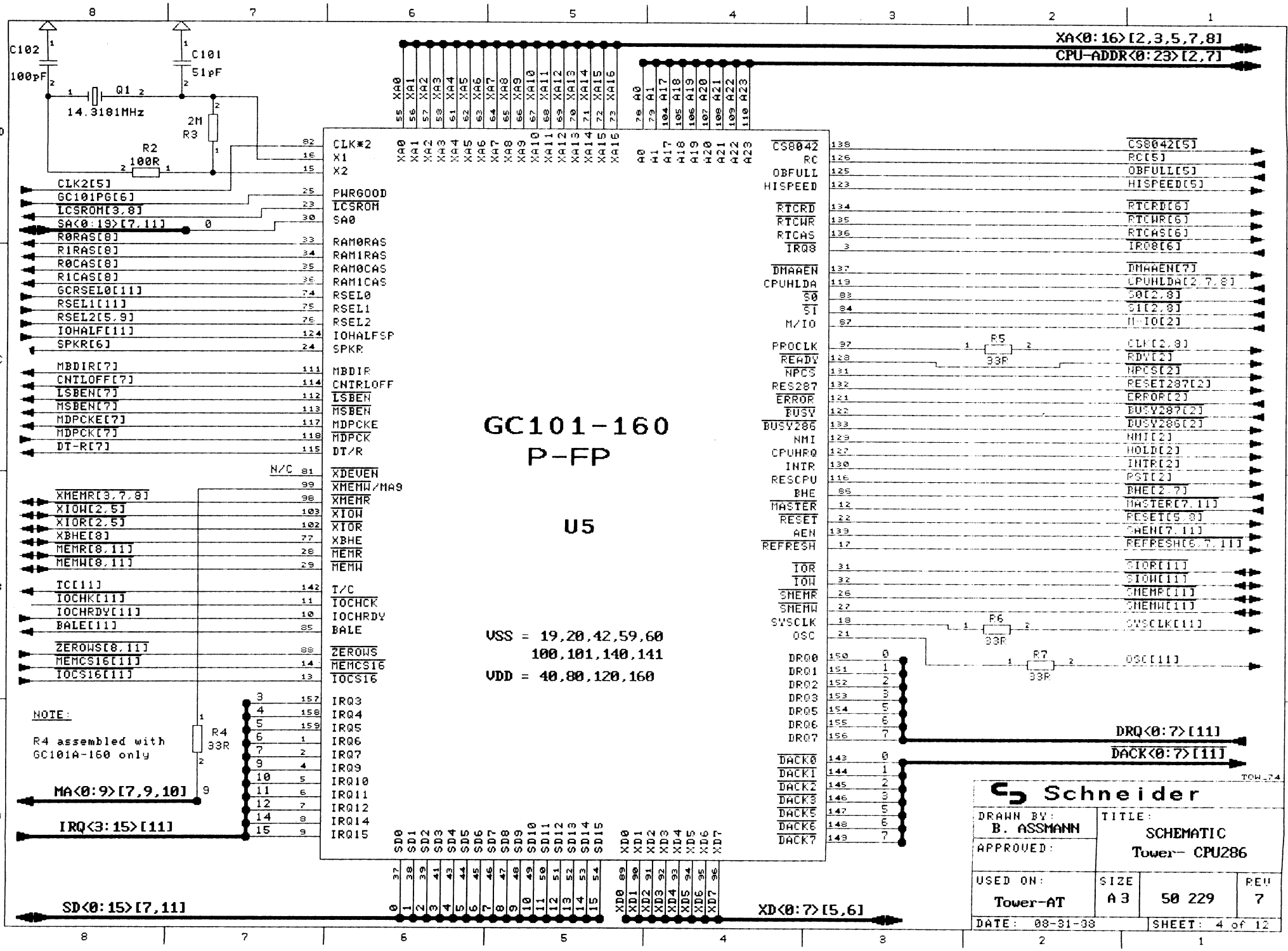


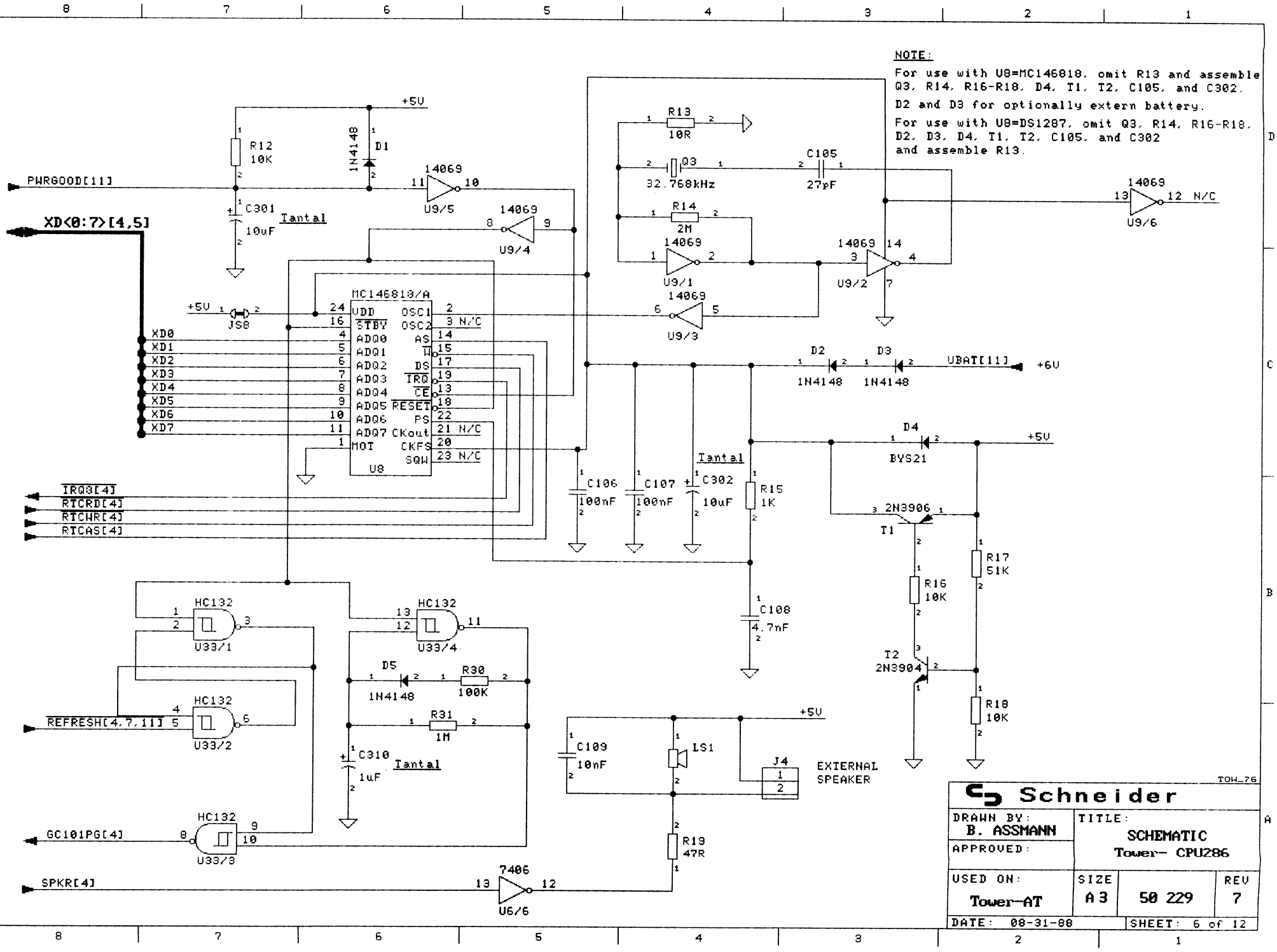
Pin assignment



Appendix A:

Different schematics CPU Rev. 8 – Rev. 7 (Layout Rev. 3)

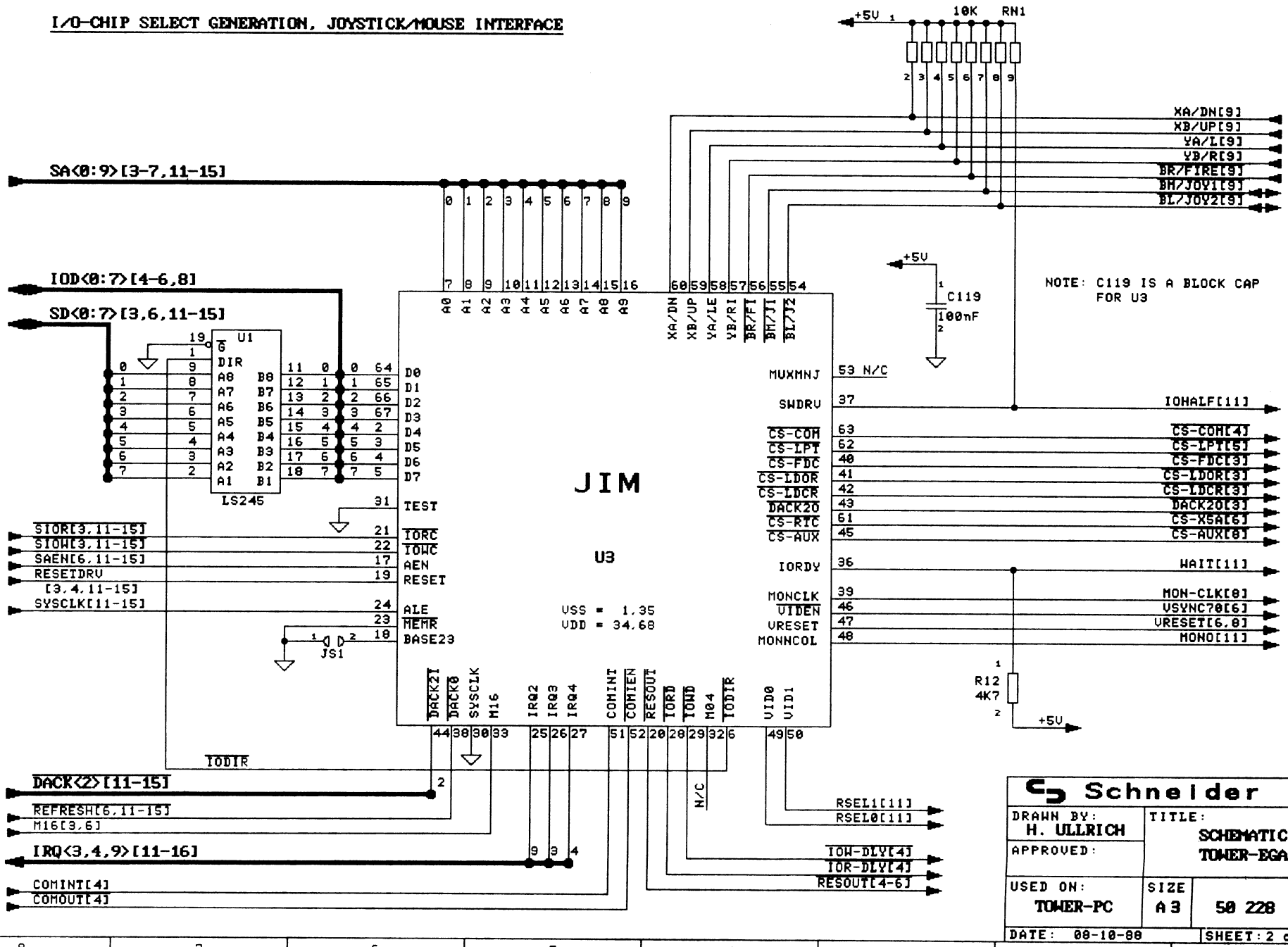

GC101-160
P-FP
U5
C102
100pF
C101
51pF
Q1
14.3181MHz
2M
R3
R2
100R
R5
33R
R6
33R
R7
33R
R4
33R
VSS = 19,20,42,59,60
100,101,140,141
VDD = 40,80,120,160
XA<0:16>[2,3,5,7,8]
CPU-ADDR<0:23>[2,7]
CLK2[5]
GC101PG[6]
LCSROM[3,8]
SA<0:19>[7,11]
R0RAS[8]
R1RAS[8]
R0CAS[8]
R1CAS[8]
GCRSEL0[11]
RSEL1[11]
RSEL2[5,9]
IOHALF[11]
SPKR[6]
MBDIR[7]
CNTLOFF[7]
LSBEN[7]
MSBEN[7]
MDPCKE[7]
MDPCK[7]
DT-R[7]
XMEMR[3,7,8]
XIOW[2,5]
XIOR[2,5]
XBHE[8]
MEMR[8,11]
MEMW[8,11]
IO[11]
IOCHK[11]
IOCHRDY[11]
BALE[11]
ZEROWS[8,11]
MEMCS16[11]
IOCS16[11]
NOTE:
R4 assembled with
GC101A-160 only
MA<0:9>[7,9,10]
IRQ<3:15>[11]
SD<0:15>[7,11]
XD<0:7>[5,6]
CS8042[5]
RC[5]
OBFULL[5]
HISPEED[5]
RTCRD[6]
RTCWR[6]
RTCAS[6]
IRQ8[6]
DMAAEN[7]
CPUHLDA[2,7,8]
S0[2,8]
S1[2,8]
M/IO[2]
CLK[2,8]
RDY[2]
NPCS[2]
RESET287[2]
ERROR[2]
BUSY287[2]
BUSY286[2]
NMI[2]
HOLD[2]
INTR[2]
RST[2]
BHE[2,7]
MASTER[7,11]
RESET[5,8]
AEN[7,11]
REFRESH[6,7,11]
IOR[11]
IOW[11]
SMEMR[11]
SMEMW[11]
SYSCLK[11]
OSC[11]
DRQ<0:7>[11]
DACK<0:7>[11]
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC Tower- CPU286
USED ON: Tower-AT
SIZE A3
50 229
REV 7
DATE: 08-31-88
SHEET: 4 of 12


NOTE:
For use with U8=MC146818, omit R13 and assemble Q3, R14, R16-R18, D4, T1, T2, C105, and C302.
D2 and D3 for optionally extern battery.
For use with U8=DS1287, omit Q3, R14, R16-R18, D2, D3, D4, T1, T2, C105, and C302 and assemble R13.
PWRGOOD[11]
XD<0:7>[4,5]
+5V
R12 10K
D1 1N4148
C301 10uF Tantal
14069 U9/5
14069 U9/4
R13 10R
Q3 32.768kHz
C105 27pF
R14 2M
14069 U9/1
14069 U9/2
14069 U9/3
14069 U9/6
MC146818/A
U8
JS8
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
D2 1N4148
D3 1N4148
UBAT[11]
+6V
D4 BYS21
C106 100nF
C107 100nF
C302 10uF Tantal
R15 1K
C108 4.7nF
IRQ8[4]
RTCRD[4]
RTCWR[4]
RTCAS[4]
2N3906 T1
R16 10K
R17 51K
T2 2N3904
R18 10K
HC132 U33/1
HC132 U33/4
HC132 U33/2
HC132 U33/3
REFRESH[4,7,11]
GC101PG[4]
D5 1N4148
R30 100K
R31 1M
C310 1uF Tantal
C109 10nF
LS1
J4
EXTERNAL SPEAKER
R19 47R
7406 U6/6
SPKR[4]
Schneider
TOW_76
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC Tower- CPU286
USED ON: Tower-AT
SIZE A3
50 229
REV 7
DATE: 08-31-88
SHEET: 6 of 12

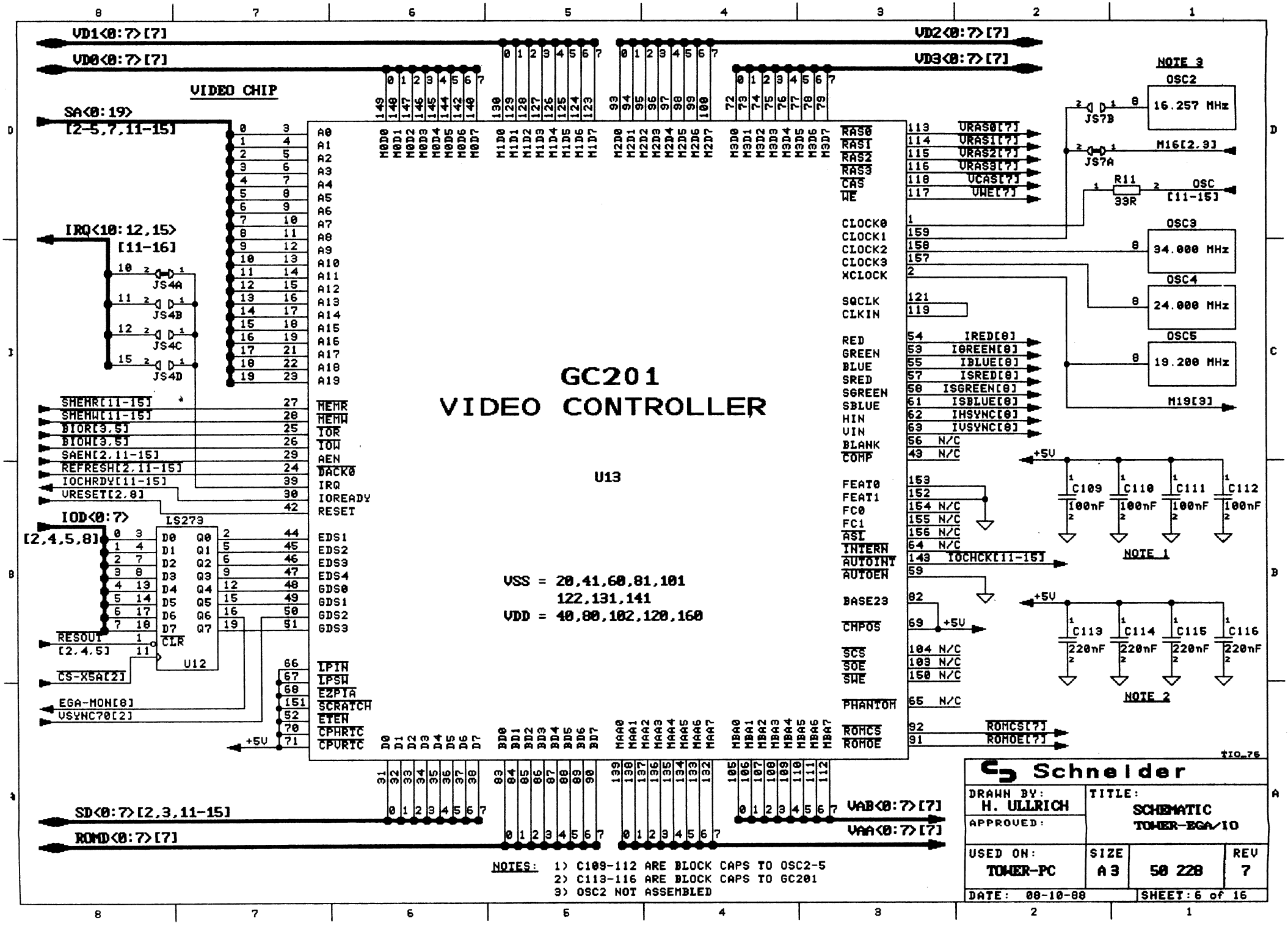
Appendix B:

Different schematics EGA I/O Rev. 8 – Rev. 7 (Layout Rev. 2 without Reworks)

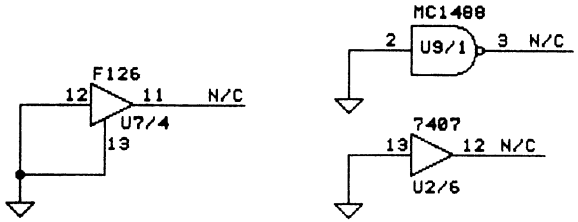
I/O-CHIP SELECT GENERATION, JOYSTICK/MOUSE INTERFACE



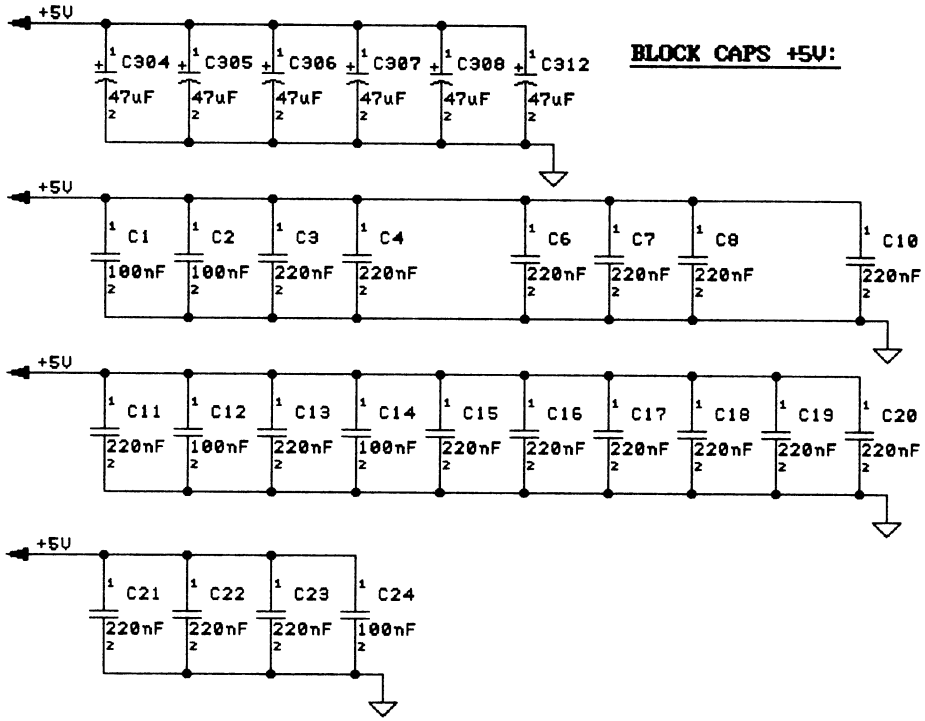
Schneider			TIO-72
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-PC	SIZE A3	50 228	REV 7
DATE: 08-10-88	SHEET: 2 of 16		

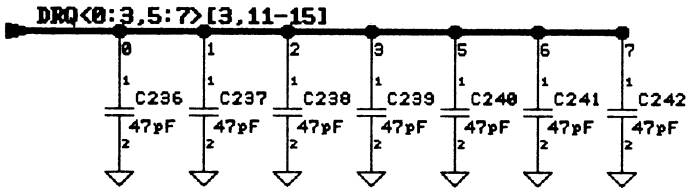

VD1<0:7>[7]
VD0<0:7>[7]
VD2<0:7>[7]
VD3<0:7>[7]
VIDEO CHIP
SA<0:19>
[2-5,7,11-15]
IRQ<10:12,15>
[11-16]
JS4A
JS4B
JS4C
JS4D
SMEMR[11-15]
SMEMW[11-15]
BIOR[3,5]
BIOW[3,5]
SAEN[2,11-15]
REFRESH[2,11-15]
IOCHRDY[11-15]
VRESET[2,8]
IOD<0:7>
[2,4,5,8]
LS273
U12
RESOUT
[2,4,5]
CS-X5A[2]
EGA-MONI[8]
VSYNC70[2]
+5V
GC201
VIDEO CONTROLLER
U13
VSS = 20,41,60,81,101
122,131,141
VDD = 40,80,102,120,160
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
MEMR
MEMW
IOR
IOW
AEN
DACK0
IRQ
IOREADY
RESET
EDS1
EDS2
EDS3
EDS4
GDS0
GDS1
GDS2
GDS3
IPIN
IPSW
E2PIA
SCRATCH
ETEN
CPHRTC
CPVRTC
RAS0
RAS1
RAS2
RAS3
CAS
WE
CLOCK0
CLOCK1
CLOCK2
CLOCK3
XCLOCK
SQCLK
CLKIN
RED
GREEN
BLUE
SRED
SGREEN
SBLUE
HIN
VIN
BLANK
COMP
FEAT0
FEAT1
FC0
FC1
ASL
INTERN
AUTOINT
AUTOEN
BASE23
CMPOS
SCS
SOE
SWE
PHANTOM
ROMCS
ROMOE
VRAS0[7]
VRAS1[7]
VRAS2[7]
VRAS3[7]
VCAS[7]
VWE[7]
IRED[8]
IGREEN[8]
IBLUE[8]
ISRED[8]
ISGREEN[8]
ISBLUE[8]
IHSYNC[8]
IVSYNC[8]
IOCHCK[11-15]
ROMCS[7]
ROMOE[7]
NOTE 3
OSC2
16.257 MHz
JS7B
JS7A
M16[2,8]
R11
33R
OSC
[11-15]
OSC3
34.000 MHz
OSC4
24.000 MHz
OSC5
19.200 MHz
M19[8]
C109
C110
C111
C112
100nF
NOTE 1
C113
C114
C115
C116
220nF
NOTE 2
SD<0:7>[2,3,11-15]
ROMD<0:7>[7]
VAB<0:7>[7]
VAA<0:7>[7]
NOTES: 1) C109-112 ARE BLOCK CAPS TO OSC2-5
2) C113-116 ARE BLOCK CAPS TO GC201
3) OSC2 NOT ASSEMBLED
Schneider
DRAWN BY: H. ULLRICH
APPROVED:
TITLE: SCHEMATIC TOWER-EGA/IO
USED ON: TOWER-PC
SIZE A3
50 228
REV 7
DATE: 08-10-88
SHEET: 6 of 16

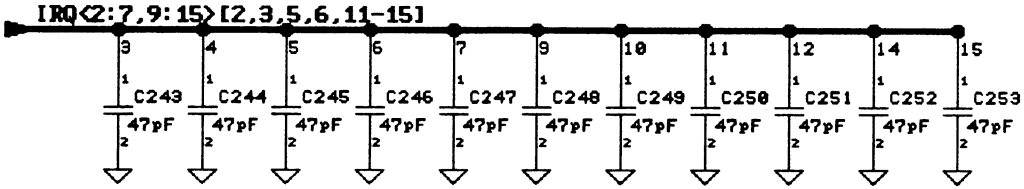
SPARE GATES



BLOCK CAPS +5V:







TIO_716

Schneider			
DRAWN BY: H. ULLRICH	TITLE: SCHEMATIC TOWER-EGA/IO		
APPROVED:			
USED ON: TOWER-PC	SIZE A3	50 228	REV 7
DATE: 08-11-88	SHEET: 16 of 16		

Appendix C:

Schematics CPU Rev. 9 (Layout Rev. 5)

REVISIONS

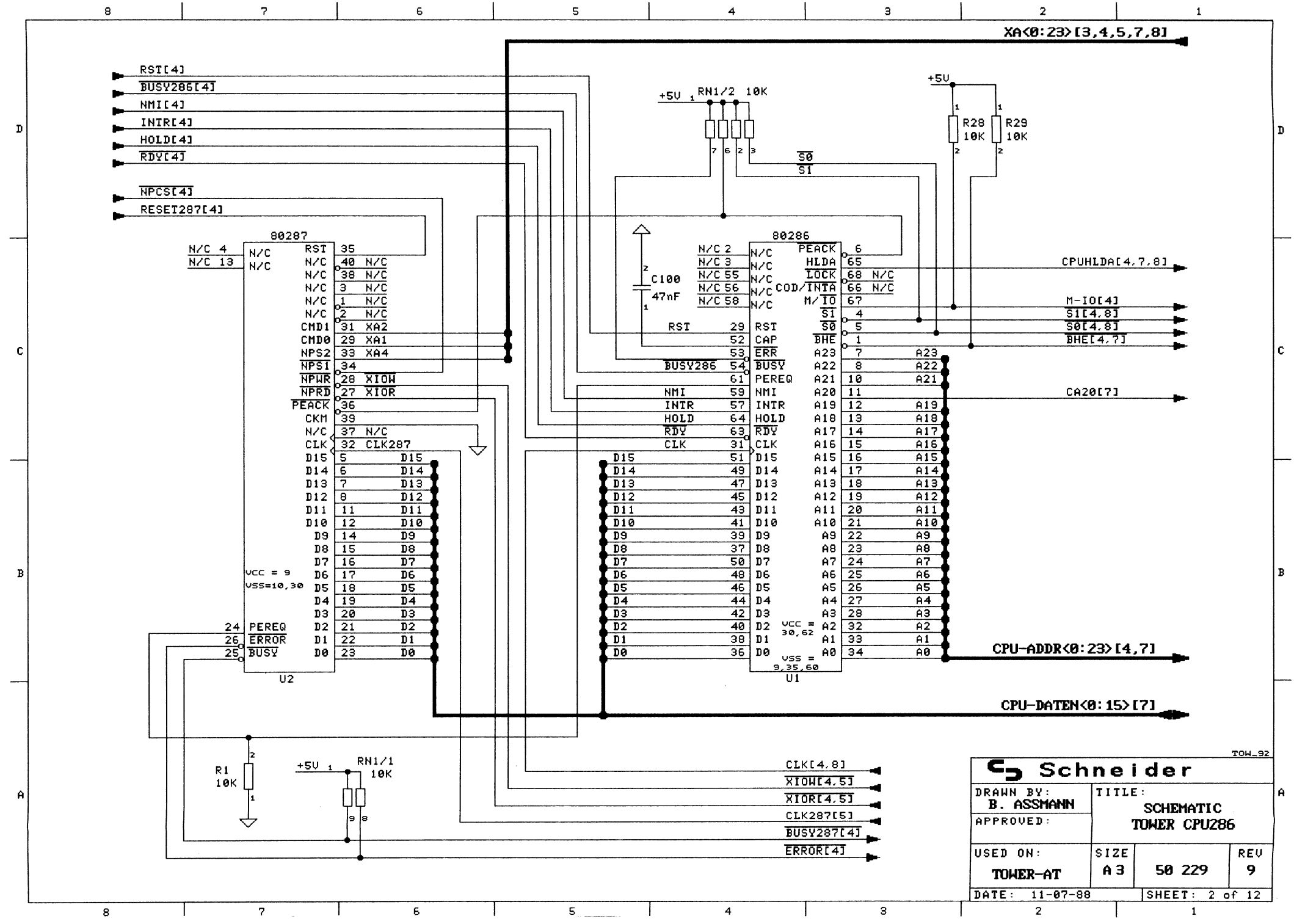
LTR	DESCRIPTION	DATE	APPROVED
1	ADVANCED ENGINEERING RELEASE	05-13-88	SCHLAGE
2		05-18-88	ASSMANN
3		06-01-88	SCHLAGE
4	First Layout	06-22-88	SCHLAGE
5	Layout REV 2	08-06-88	ASSMANN
6	Layout REV 2 CORRECTIONS	08-22-88	ASSMANN
7	PCB REV 2A FIX OF BUS '/MASTER'	08-31-88	ASSMANN
8	PCB REV 4. LAYOUT: ADDITIONAL RESET LOGIC ELIMINATED	11-02-88	ULLRICH
9	PCB REV 5. LAYOUT: WITH GC 101 D	11-07-88	ASSMANN

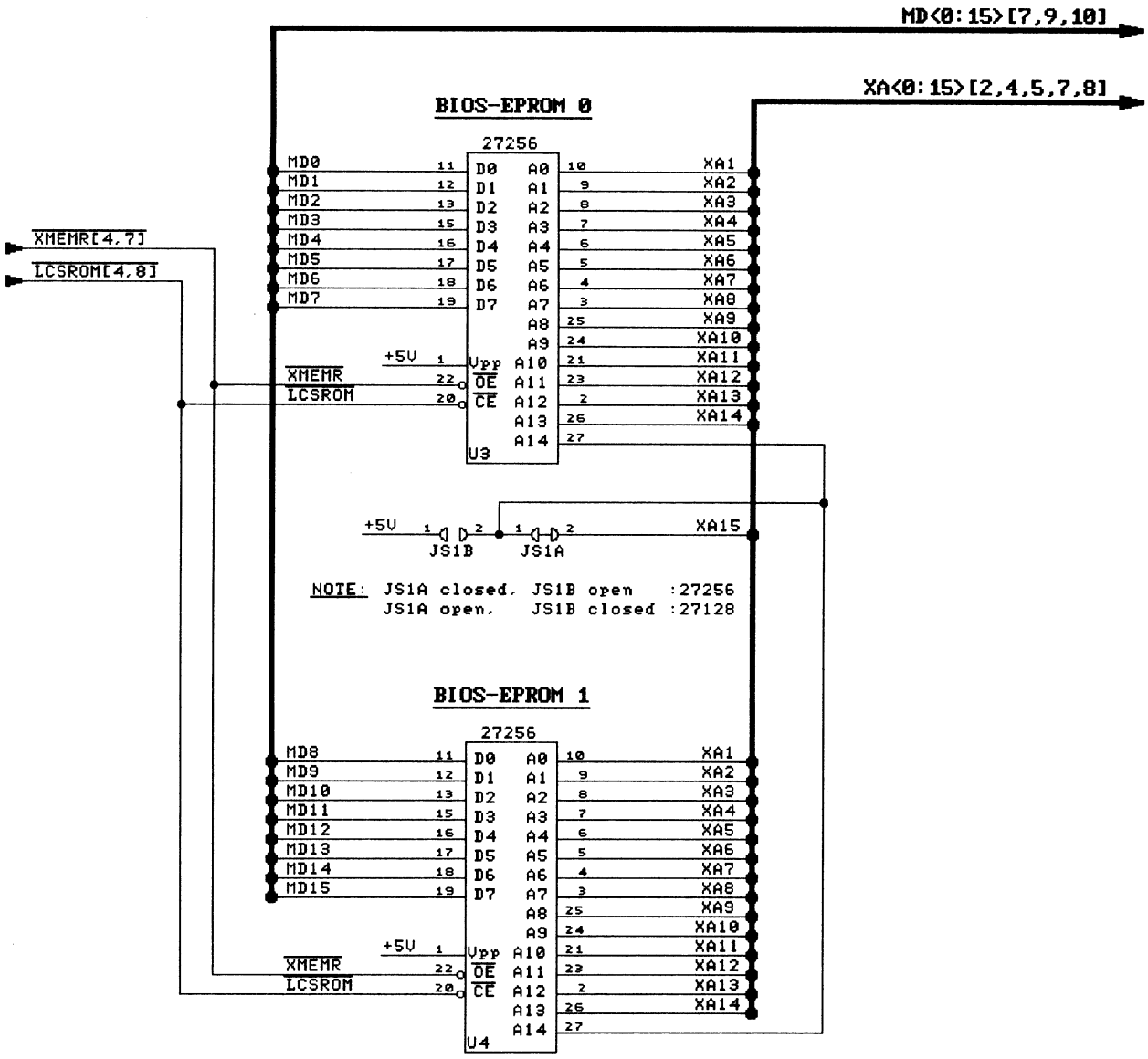
DRAWING FILES:	CONTENTS:
TOW_91.DWG	THIS SHEET
TOW_92.DWG	CPU SECTION
TOW_93.DWG	BIOS EPROMS
TOW_94.DWG	GC 101 D
TOW_95.DWG	KEYBOARD / CLOCKS
TOW_96.DWG	REAL TIME CLOCK
TOW_97.DWG	ADDRESS / DATA BUFFERS
TOW_98.DWG	TIMING FOR MEMORY
TOW_99.DWG	MEMORY ON SIL- MODULE
TOW_910.DWG	MEMORY ON BOARD
TOW_911.DWG	CONNECTORS
TOW_912.DWG	BLOCK CAPS

TOW_91

Schneider

DRAWN BY: B. ASSMANN	TITLE: SCHEMATICS TOWER CPU286		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 229	REV 9
DATE: 11-07-88	SHEET: 1 of 12		

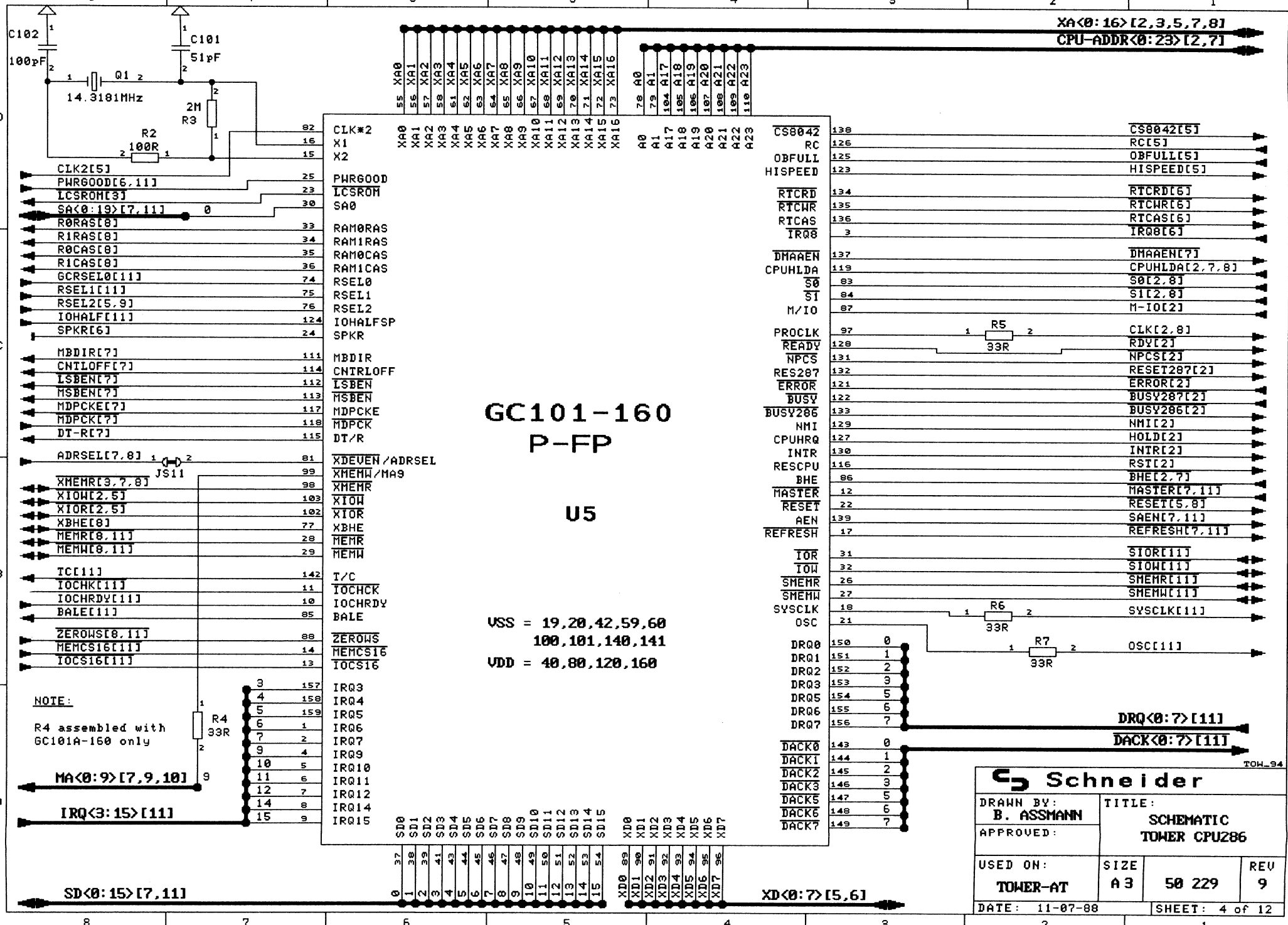

XA<0:23>[3,4,5,7,8]
RST[4]
BUSY286[4]
NMI[4]
INTR[4]
HOLD[4]
RDY[4]
NPCS[4]
RESET287[4]
80287
80286
U2
U1
RN1/2 10K
RN1/1 10K
R1 10K
R28 10K
R29 10K
C100 47nF
+5V
S0
S1
VCC = 9
VSS=10,30
VCC = 30,62
VSS = 9,35,60
CPUHLDA[4,7,8]
M-IO[4]
S1[4,8]
S0[4,8]
BHE[4,7]
CA20[7]
CPU-ADDR<0:23>[4,7]
CPU-DATEN<0:15>[7]
CLK[4,8]
XIOW[4,5]
XIOR[4,5]
CLK287[5]
BUSY287[4]
ERROR[4]
TOW_92
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 2 of 12

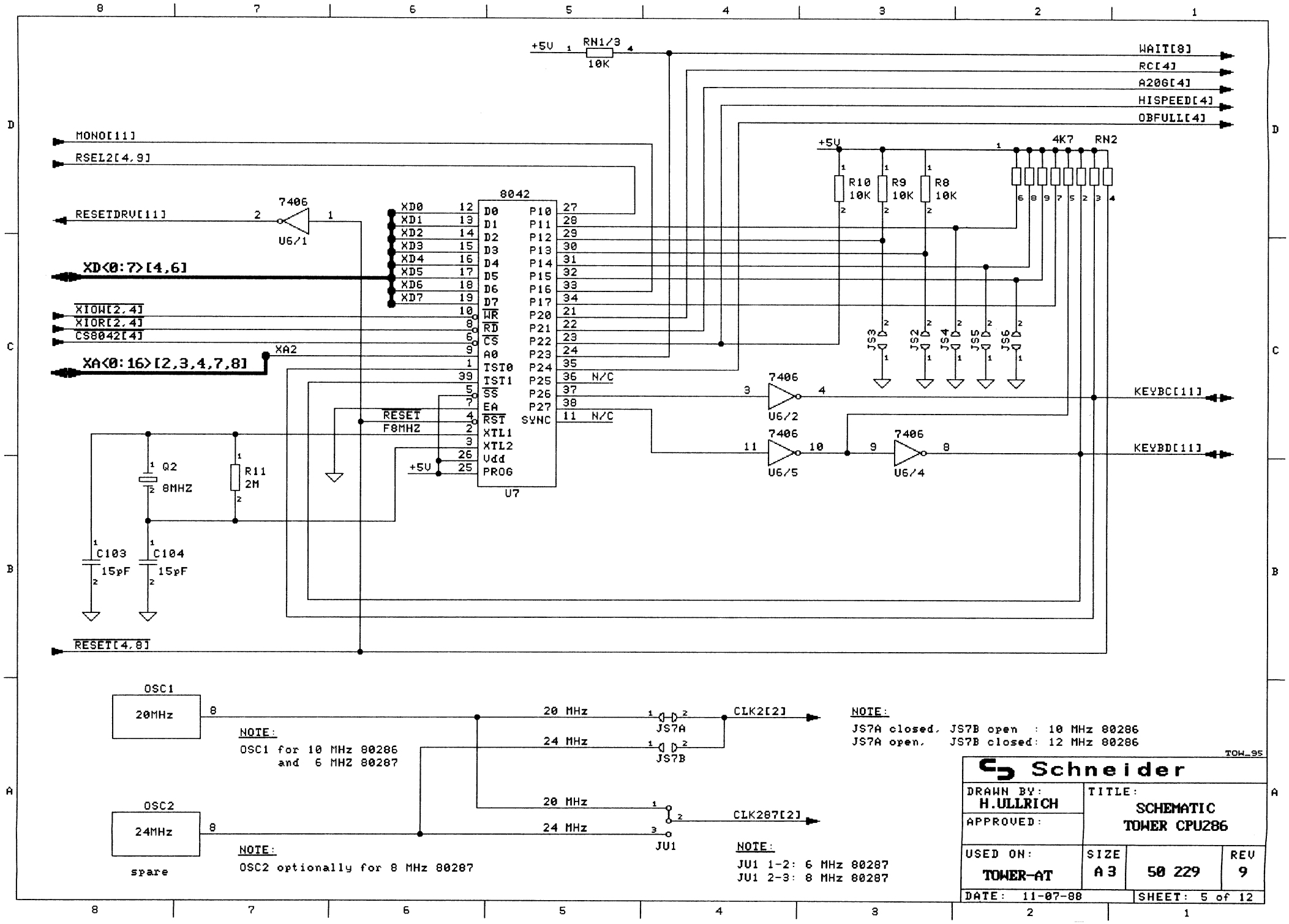


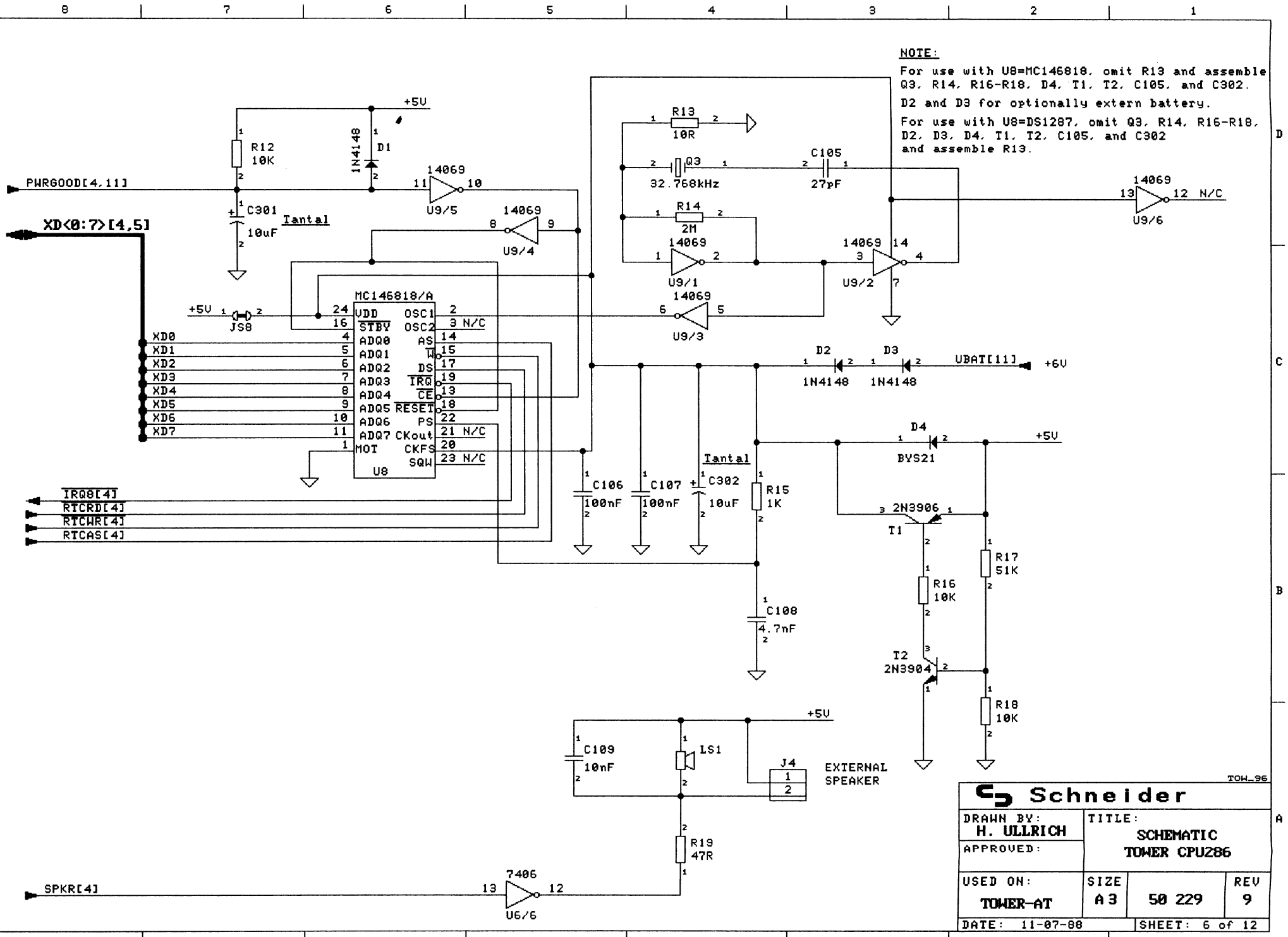
TOW_93

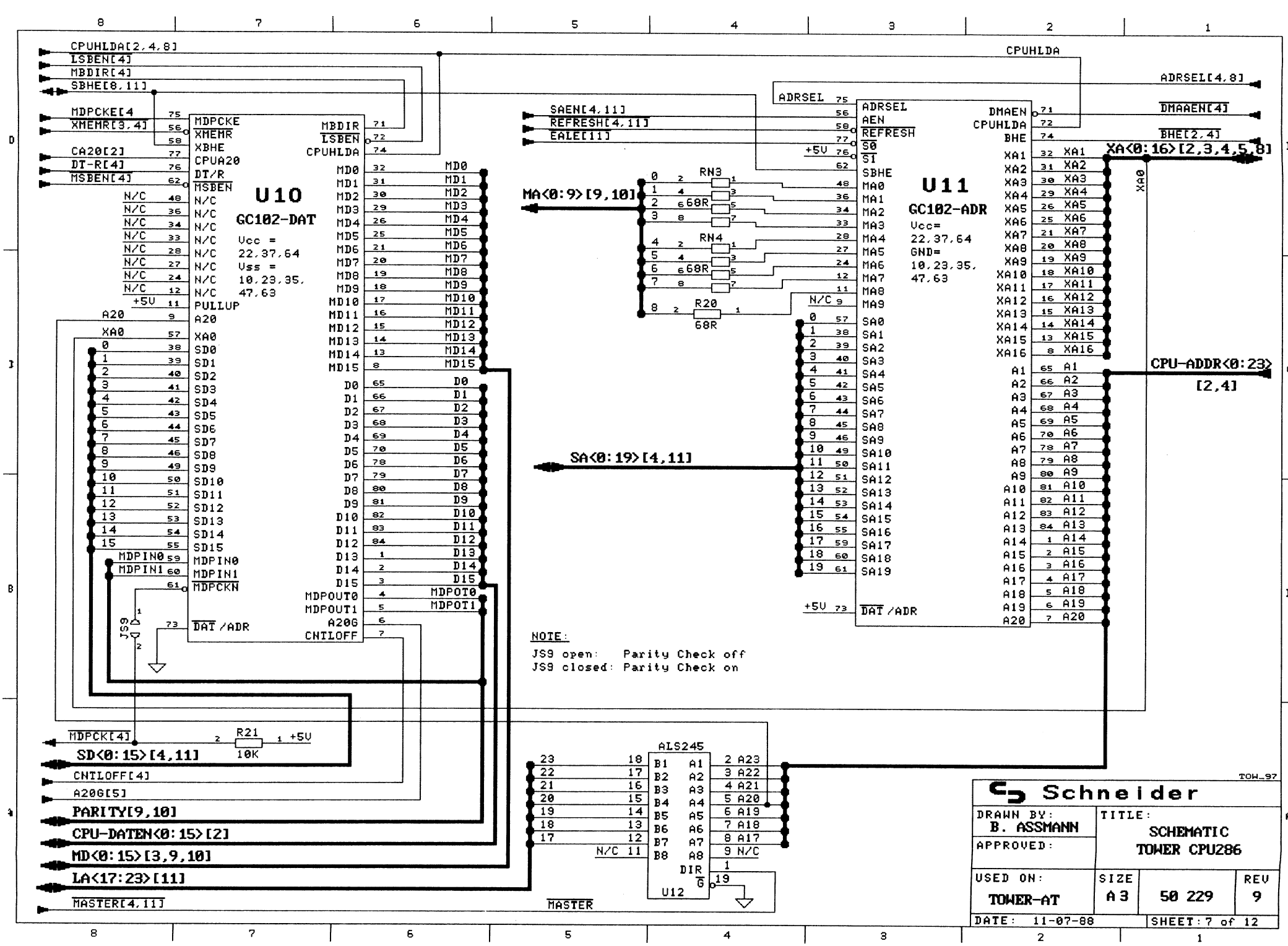
Schneider

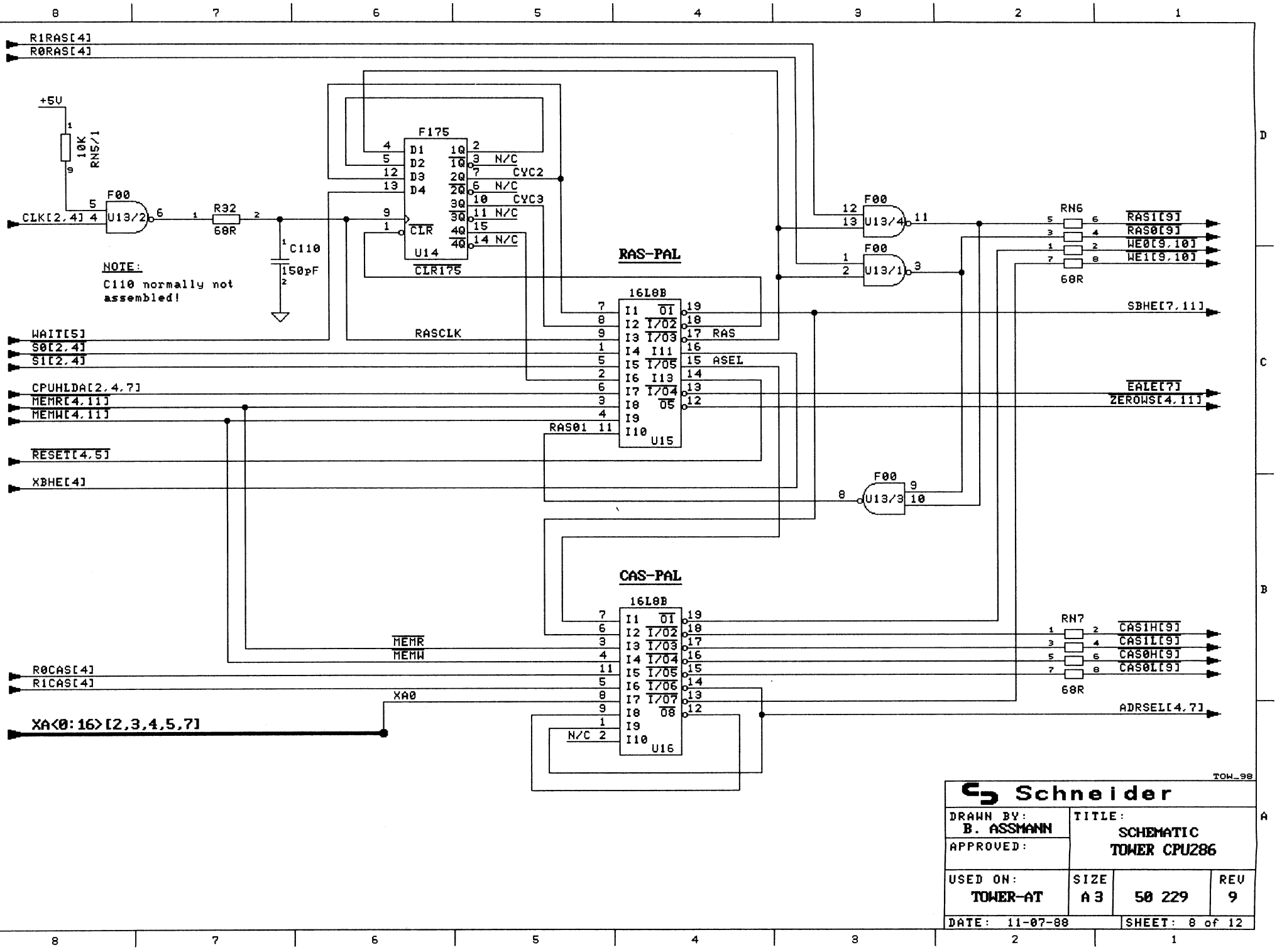
DRAWN BY: B.ASSMANN	TITLE: SCHEMATIC TOWER CPU286		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 229	REV 9
DATE: 11-07-88	SHEET: 3 of 12		

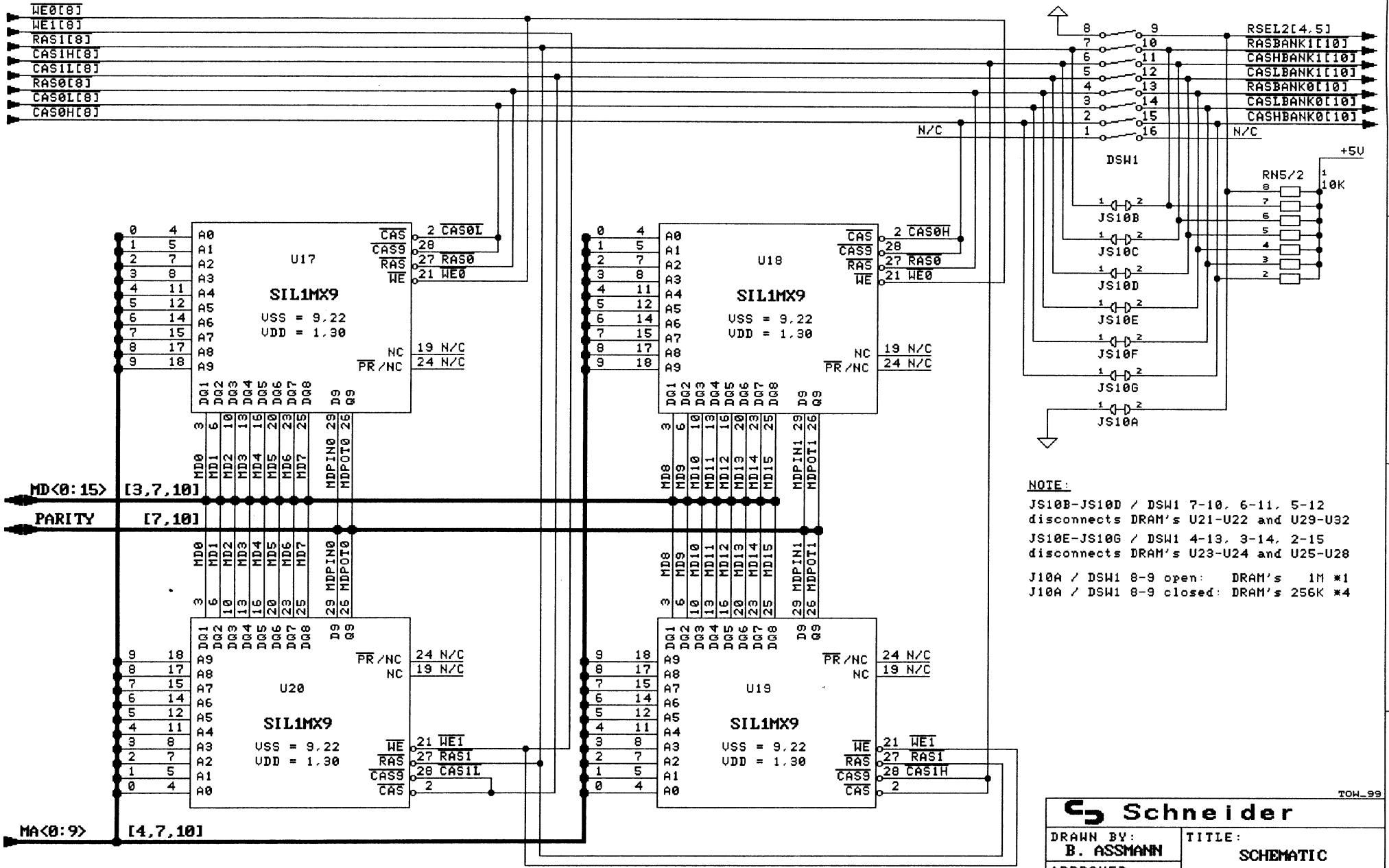

C102
100pF
C101
51pF
Q1
14.3181MHz
2M
R3
R2
100R
R4
33R
R5
33R
R6
33R
R7
33R
JS11
GC101-160
P-FP
U5
VSS = 19,20,42,59,60
100,101,140,141
VDD = 40,80,120,160
XA<0:16>[2,3,5,7,8]
CPU-ADDR<0:23>[2,7]
CLK2[5]
PWRGOOD[6,11]
LCSROM[3]
SA<0:19>[7,11]
R0RAS[8]
R1RAS[8]
R0CAS[8]
R1CAS[8]
GCRSEL0[11]
RSEL1[11]
RSEL2[5,9]
IOHALF[11]
SPKR[6]
MBDIR[7]
CNTLOFF[7]
LSBEN[7]
MSBEN[7]
MDPCKE[7]
MDPCK[7]
DT-R[7]
ADRSEL[7,8]
XMEMR[3,7,8]
XIOW[2,5]
XIOR[2,5]
XBHE[8]
MEMR[8,11]
MEMW[8,11]
TC[11]
IOCHK[11]
IOCHRDY[11]
BALE[11]
ZEROWS[8,11]
MEMCS16[11]
IOCS16[11]
NOTE:
R4 assembled with
GC101A-160 only
MA<0:9>[7,9,10]
IRQ<3:15>[11]
SD<0:15>[7,11]
XD<0:7>[5,6]
CS8042[5]
RC[5]
OBFULL[5]
HISPEED[5]
RTCRD[6]
RTCWR[6]
RTCAS[6]
IRQ8[6]
DMAAEN[7]
CPUHLDA[2,7,8]
S0[2,8]
S1[2,8]
M-IO[2]
CLK[2,8]
RDY[2]
NPCS[2]
RESET287[2]
ERROR[2]
BUSY287[2]
BUSY286[2]
NMI[2]
HOLD[2]
INTR[2]
RST[2]
BHE[2,7]
MASTER[7,11]
RESET[5,8]
SAEN[7,11]
REFRESH[7,11]
SIOR[11]
SIOW[11]
SMEMR[11]
SMEMW[11]
SYSCLK[11]
OSC[11]
DRQ<0:7>[11]
DACK<0:7>[11]
TOW_94
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 4 of 12

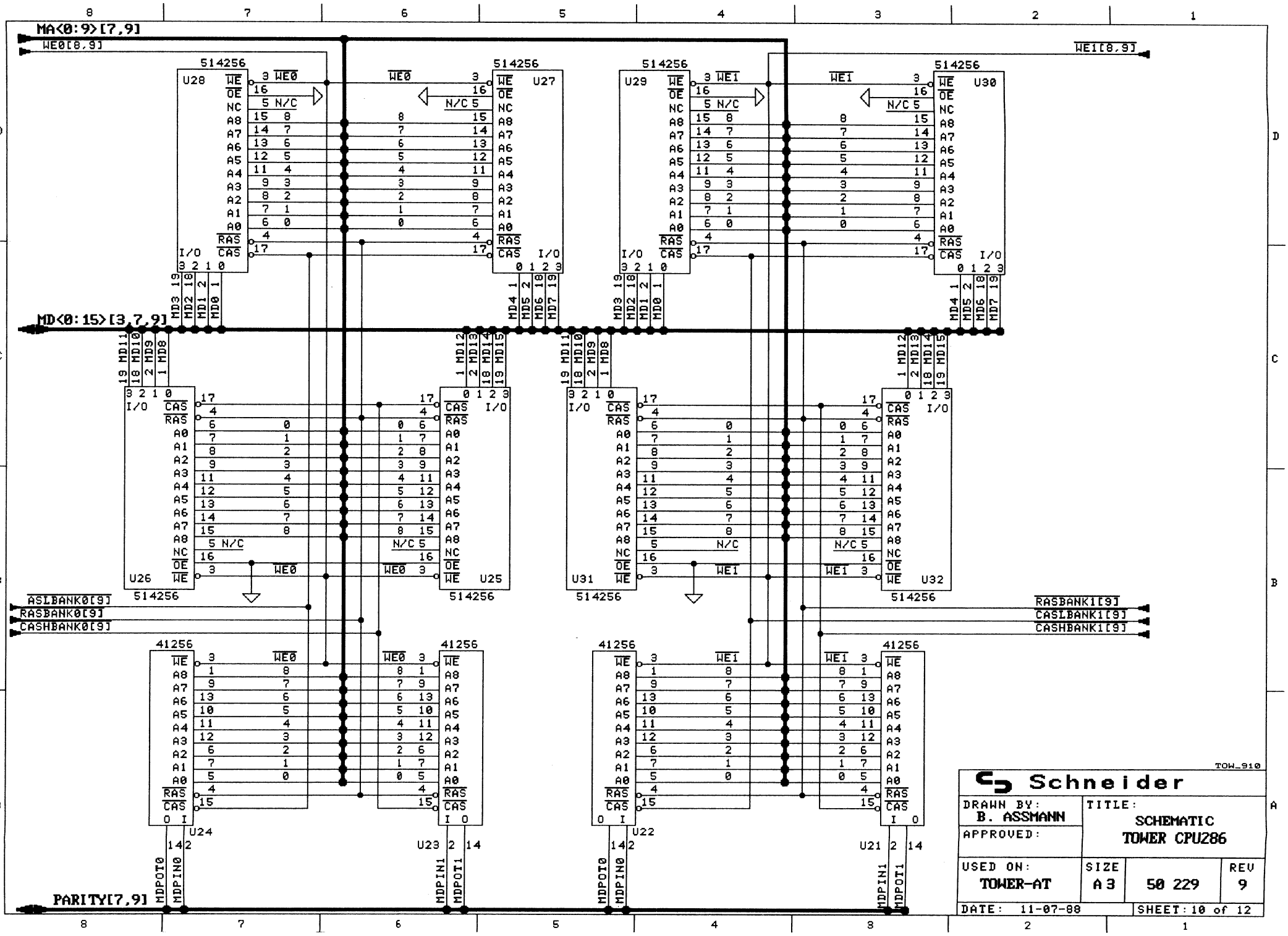

+5V
RN1/3
10K
WAIT[8]
RC[4]
A20G[4]
HISPEED[4]
OBFULL[4]
MONO[11]
RSEL2[4,9]
RESETDRV[11]
7406
U6/1
8042
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
D0
D1
D2
D3
D4
D5
D6
D7
P10
P11
P12
P13
P14
P15
P16
P17
XD<0:7>[4,6]
XIOW[2,4]
XIOR[2,4]
CS8042[4]
XA<0:16>[2,3,4,7,8]
XA2
WR
RD
CS
A0
TST0
TST1
SS
EA
RST
SYNC
P20
P21
P22
P23
P24
P25
P26
P27
N/C
RESET
F8MHZ
XTL1
XTL2
Vdd
PROG
U7
R10
R9
R8
10K
4K7
RN2
JS3
JS2
JS4
JS5
JS6
7406
U6/2
U6/5
U6/4
KEYBC[11]
KEYBD[11]
Q2
8MHZ
R11
2M
C103
C104
15pF
RESET[4,8]
OSC1
20MHz
NOTE:
OSC1 for 10 MHz 80286
and 6 MHz 80287
20 MHz
24 MHz
JS7A
JS7B
CLK2[2]
NOTE:
JS7A closed, JS7B open : 10 MHz 80286
JS7A open, JS7B closed: 12 MHz 80286
OSC2
24MHz
spare
NOTE:
OSC2 optionally for 8 MHz 80287
JU1
CLK287[2]
NOTE:
JU1 1-2: 6 MHz 80287
JU1 2-3: 8 MHz 80287
TOW_95
Schneider
DRAWN BY: H.ULLRICH
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 5 of 12

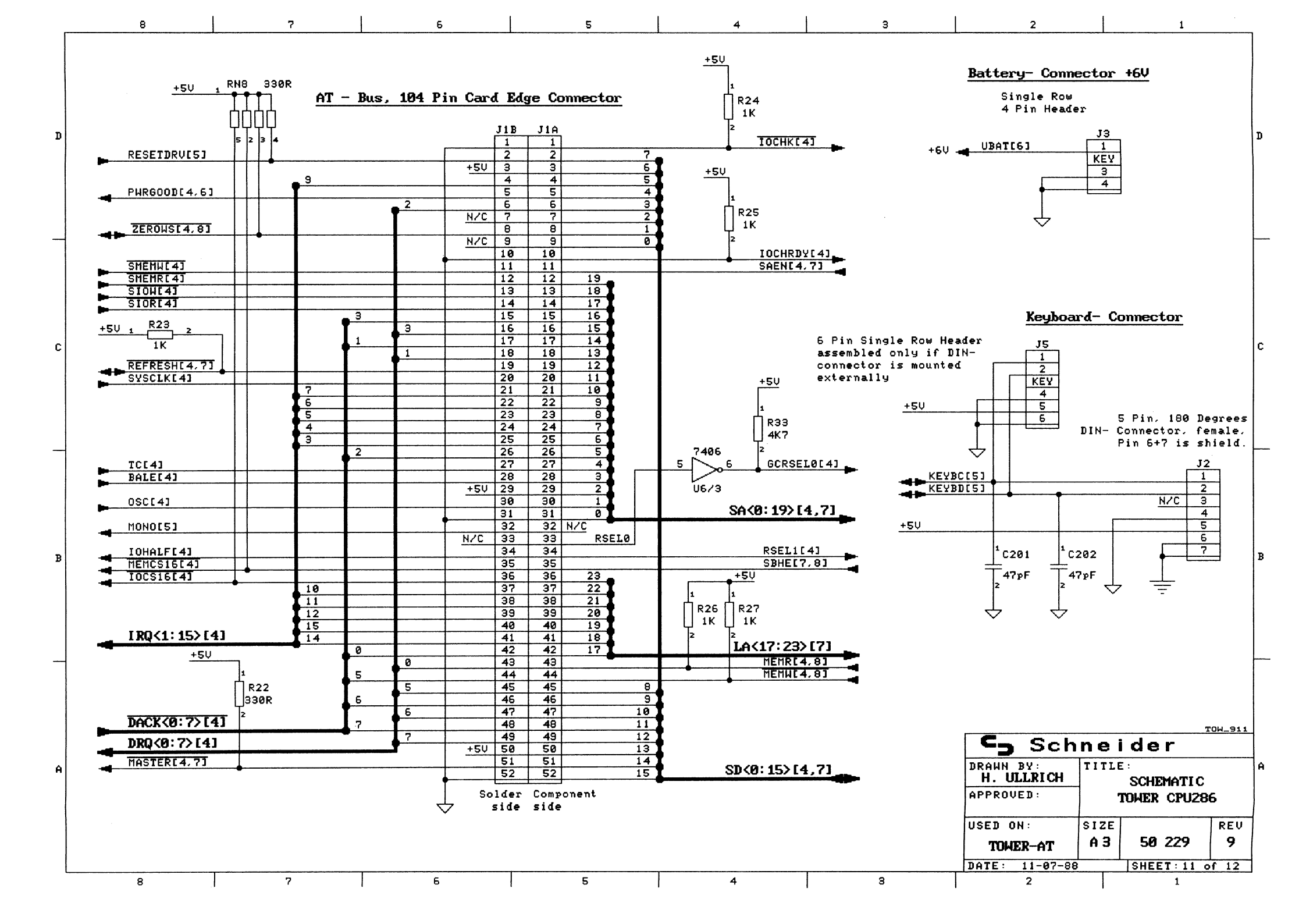

NOTE:
For use with U8=MC146818, omit R13 and assemble Q3, R14, R16-R18, D4, T1, T2, C105, and C302.
D2 and D3 for optionally extern battery.
For use with U8=DS1287, omit Q3, R14, R16-R18, D2, D3, D4, T1, T2, C105, and C302 and assemble R13.
+5V
R12 10K
1N4148
D1
PWRGOOD[4,11]
14069
U9/5
C301 10uF Tantal
XD<0:7>[4,5]
U9/4
MC146818/A
U8
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
IRQ8[4]
RTCRD[4]
RTCWR[4]
RTCAS[4]
JS8
R13 10R
Q3 32.768kHz
C105 27pF
R14 2M
U9/1
U9/2
U9/3
U9/6
N/C
D2 1N4148
D3 1N4148
UBAT[11]
+6V
D4 BYS21
C106 100nF
C107 100nF
C302 10uF Tantal
R15 1K
C108 4.7nF
T1 2N3906
T2 2N3904
R16 10K
R17 51K
R18 10K
C109 10nF
LS1
J4
EXTERNAL SPEAKER
R19 47R
SPKR[4]
7406
U6/6
TOW_96
Schneider
DRAWN BY: H. ULLRICH
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 6 of 12

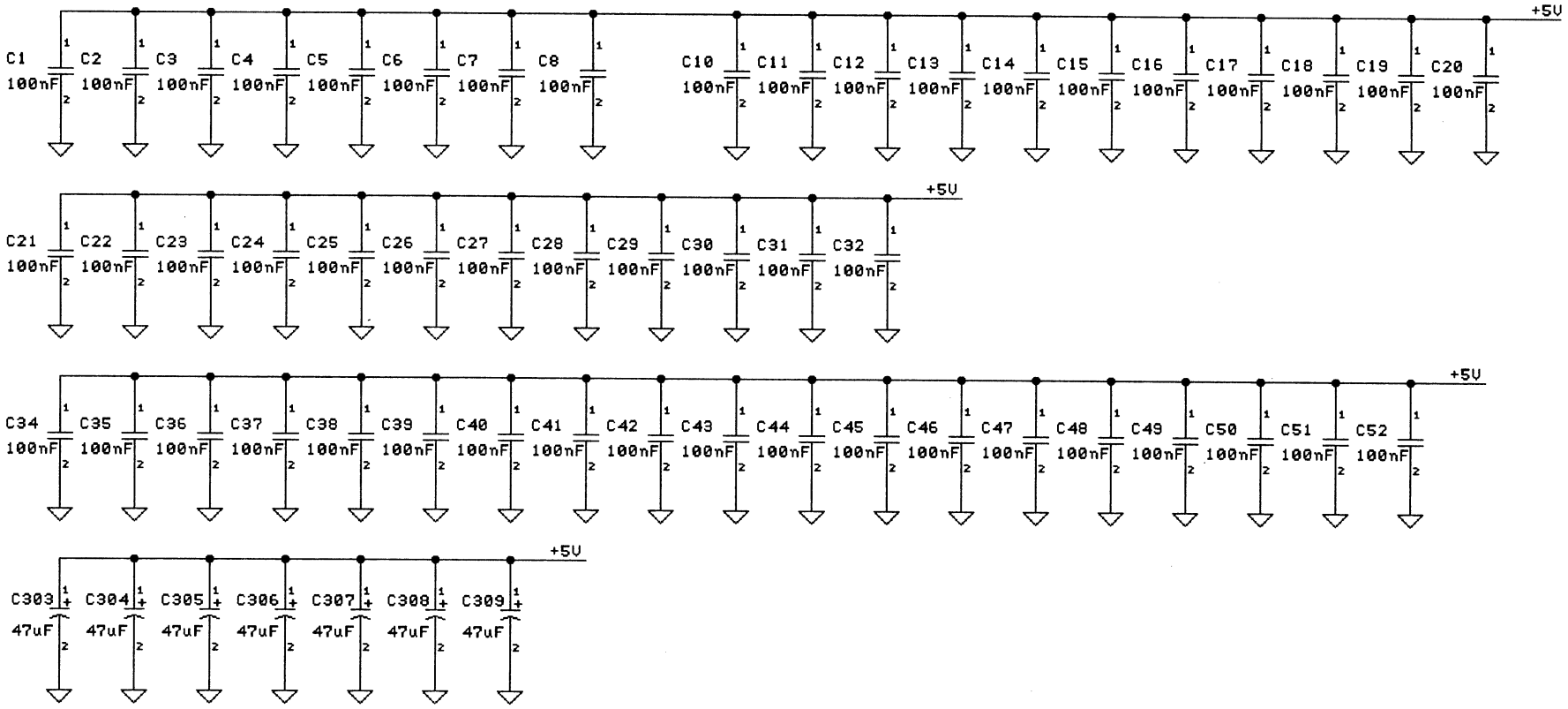

CPUHLDA[2,4,8]
LSBEN[4]
MBDIR[4]
SBHE[8,11]
MDPCKE[4
XMEMR[3,4]
CA20[2]
DT-R[4]
MSBEN[4]
U10
GC102-DAT
Vcc = 22,37,64
Vss = 10,23,35, 47,63
PULLUP
MDPCKE
XMEMR
XBHE
CPUA20
DT/R
MSBEN
MBDIR
LSBEN
CPUHLDA
A20
XA0
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
MDPIN0
MDPIN1
MDPCKN
DAT/ADR
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
MDPOUT0
MDPOUT1
A20G
CNILOFF
JS9
MDPCK[4]
R21
10K
+5V
SD<0:15>[4,11]
CNILOFF[4]
A20G[5]
PARITY[9,10]
CPU-DATEN<0:15>[2]
MD<0:15>[3,9,10]
LA<17:23>[11]
MASTER[4,11]
SAEN[4,11]
REFRESH[4,11]
EALE[11]
MA<0:9>[9,10]
RN3
RN4
68R
R20
68R
SA<0:19>[4,11]
U11
GC102-ADR
Vcc= 22,37,64
GND= 10,23,35, 47,63
ADRSEL
AEN
REFRESH
S0
S1
SBHE
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
DAT/ADR
DMAEN
CPUHLDA
BHE
XA1
XA2
XA3
XA4
XA5
XA6
XA7
XA8
XA9
XA10
XA11
XA12
XA13
XA14
XA15
XA16
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
ALS245
U12
DIR
G
ADRSEL[4,8]
DMAAEN[4]
BHE[2,4]
XA<0:16>[2,3,4,5,8]
CPU-ADDR<0:23>
[2,4]
NOTE:
JS9 open: Parity Check off
JS9 closed: Parity Check on
Schneider
TOW_97
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 7 of 12


R1RAS[4]
R0RAS[4]
+5V
10K
RN5/1
F00
U13/2
CLK[2,4]
R32
68R
C110
150pF
NOTE:
C110 normally not assembled!
F175
U14
CLR175
CYC2
CYC3
N/C
RASCLK
RAS-PAL
16L8B
U15
RAS
ASEL
RAS01
WAIT[5]
S0[2,4]
S1[2,4]
CPUHLDA[2,4,7]
MEMR[4,11]
MEMW[4,11]
RESET[4,5]
XBHE[4]
U13/4
U13/1
U13/3
RN6
RAS1[9]
RAS0[9]
WE0[9,10]
WE1[9,10]
SBHE[7,11]
EALE[7]
ZEROWS[4,11]
CAS-PAL
U16
MEMR
MEMW
R0CAS[4]
R1CAS[4]
XA0
XA<0:16>[2,3,4,5,7]
RN7
CAS1H[9]
CAS1L[9]
CAS0H[9]
CAS0L[9]
ADRSEL[4,7]
TOW_98
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 8 of 12


WE0[8]
WE1[8]
RAS1[8]
CAS1H[8]
CAS1L[8]
RAS0[8]
CAS0L[8]
CAS0H[8]
N/C
RSEL2[4,5]
RASBANK1[10]
CASHBANK1[10]
CASLBANK1[10]
RASBANK0[10]
CASLBANK0[10]
CASHBANK0[10]
N/C
DSW1
+5V
RN5/2
10K
JS10B
JS10C
JS10D
JS10E
JS10F
JS10G
JS10A
U17
U18
U19
U20
SIL1MX9
VSS = 9.22
VDD = 1.30
CAS
CAS9
RAS
WE
NC
PR/NC
2 CAS0L
2 CAS0H
27 RAS0
21 WE0
19 N/C
24 N/C
MD<0:15> [3,7,10]
PARITY [7,10]
MA<0:9> [4,7,10]
MDPIN0
MDPOT0
MDPIN1
MDPOT1
21 WE1
27 RAS1
28 CAS1L
28 CAS1H
2
NOTE:
JS10B-JS10D / DSW1 7-10, 6-11, 5-12
disconnects DRAM's U21-U22 and U29-U32
JS10E-JS10G / DSW1 4-13, 3-14, 2-15
disconnects DRAM's U23-U24 and U25-U28
J10A / DSW1 8-9 open: DRAM's 1M *1
J10A / DSW1 8-9 closed: DRAM's 256K *4
TOW_99
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 9 of 12


MA<0:9>[7,9]
WE0[8,9]
WE1[8,9]
MD<0:15>[3,7,9]
514256
U28
U27
U29
U30
U26
U25
U31
U32
41256
U24
U23
U22
U21
ASLBANK0[9]
RASBANK0[9]
CASHBANK0[9]
RASBANK1[9]
CASLBANK1[9]
CASHBANK1[9]
MDPOT0
MDPIN0
MDPIN1
MDPOT1
PARITY[7,9]
TOW_910
Schneider
DRAWN BY: B. ASSMANN
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 10 of 12


AT - Bus, 104 Pin Card Edge Connector
Battery- Connector +6V
Single Row
4 Pin Header
Keyboard- Connector
6 Pin Single Row Header
assembled only if DIN-
connector is mounted
externally
5 Pin, 180 Degrees
DIN- Connector, female,
Pin 6+7 is shield.
RESETDRV[5]
PWRGOOD[4,6]
ZEROWS[4,8]
SMEMW[4]
SMEMR[4]
SIOW[4]
SIOR[4]
REFRESH[4,7]
SYSCLK[4]
TC[4]
BALE[4]
OSC[4]
MONO[5]
IOHALF[4]
MEMCS16[4]
IOCS16[4]
IRQ<1:15>[4]
DACK<0:7>[4]
DRQ<0:7>[4]
MASTER[4,7]
IOCHK[4]
IOCHRDY[4]
SAEN[4,7]
SA<0:19>[4,7]
RSEL0
RSEL1[4]
SBHE[7,8]
LA<17:23>[7]
MEMR[4,8]
MEMW[4,8]
SD<0:15>[4,7]
GCRSEL0[4]
UBAT[6]
KEYBC[5]
KEYBD[5]
Solder side
Component side
Schneider
TOW_911
DRAWN BY: H. ULLRICH
APPROVED:
TITLE: SCHEMATIC TOWER CPU286
USED ON: TOWER-AT
SIZE A3
50 229
REV 9
DATE: 11-07-88
SHEET: 11 of 12



TOW_912

Schneider

DRAWN BY: B. ASSMANN	TITLE: SCHEMATIC TOWER CPU286		
APPROVED:			
USED ON: TOWER-AT	SIZE A3	50 229	REV 9
DATE: 11-07-88	SHEET: 12 of 12		

Bitte bei Ersatzteilbestellung die genaue Bezeichnung und Ident-Nr. (siehe Typenschild) des Gerätes sowie Bestell-Nummer und Positions-Nummer des Ersatzteils angeben.

For ordering of spare parts please state exact description and ident.-no. of unit (see silver rating label on the backside of unit) as well as part no. and position no. of required spare parts.

Benutzen Sie:

Telex: 531516

oder

*317298 #

oder

Telefax: 08245/51326